ID	Title
1002	An Efficient Kriging-based Constrained Multi-objective Evolutionary Algorithm for Analog Circuit Synthesis via Self-adaptive Incremental Learning
1010	HEALM: Hardware-Efficient Approximate Logarithmic Multiplier with Reduced Error
1011	FeMIC: Multi-Operands In-Memory Computing Based on FeFETs
1012	Solving Least-Squares Fitting in O(1) Using RRAM-based Computing-in-Memory Technique
1013	Optimal Data Allocation for Graph Processing in Processing-in-Memory Systems
1014	Automated Detection of Spatial Memory Safety Violations for Constrained Devices
1015	Efficient Computer Vision on Edge Devices with Pipeline-Parallel Hierarchical Neural Networks
1016	RADARS: Memory Efficient Reinforcement Learning Aided Differentiable Neural Architecture Search
1020	TENET: Temporal CNN with Attention for Network Anomaly Detection in Automotive Cyber-Physical Systems
1021	Accelerate SAT-based ATPG via Preprocessing and New Conflict Management Heuristics
1025	SONIC: A Sparse Neural Network Inference Accelerator with Silicon Photonics for Energy-Efficient Deep Learning
1030	Sparsity-Aware Non-Volatile Computing-In-Memory Macro with Analog Switch Array and Low-Resolution Current-Mode ADC
1031	FIRVER: Concolic Testing for Systematic Validation of Firmware Binaries
1034	Fast Variation-aware Circuit Sizing Approach for Analog Design with ML-Assisted Evolutionary Algorithm
1038	Fortify: Analytical Pre-Silicon Side-Channel Characterization of Digital Designs
1040	Generalizing Tandem Simulation: Connecting High-level and RTL Simulation Models
1041	DistriHD: A Memory Efficient Distributed Binary Hyperdimensional Computing Architecture for Image Classification
1045	TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture
1050	Toward Optical Probing Resistant Circuits: A Comparison of Logic Styles and Circuit Design Techniques
1052	PUMP: Profiling-free Unified Memory Prefetcher for Large DNN Model Support
1054	Limiting the Search Space in Optimal Quantum Circuit Mapping
1058	Neural Network Pruning and Fast Training for DRL-based UAV Trajectory Planning
1060	A Novel and Efficient Bayesian Optimization Approach for Analog Designs with Multi-Testbench
1064	ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement
1065	Vector-based Dynamic IR-drop Prediction Using Machine Learning
1068	Mapping Large Scale Finite Element Computing onto Wafer-Scale Engines
1069	OpenHD: An Efficient GPU-Powered Framework for Hyperdimensional Computing
1071	A Graph Neural Network Method for Fast ECO Leakage Power Optimization
1073	Pre-Routing Path Delay Estimation Based on Transformer and Residual Framework
1074	Efficient Routing for Coarse-Grained Reconfigurable Arrays using Multi-Pole NEM Relays
1085	Fault Testing and Diagnosis Techniques for Carbon Nanotube-Based FPGAs
1087	SonicFFT: A system architecture for ultrasonic-based FFT acceleration
1088	Efficient Preparation of Cyclic Quantum States

1092	HAWIS: Hardware-Aware Automated WIdth Search for Accurate, Energy-Efficient and Robust Binary Neural Network on ReRAM Dot-Product Engine
1098	Side-channel attacks on Kyber-A NIST PQC final candidate
1099	Improving the Robustness of Microfluidic Networks
1104	Thermal-aware Layout Optimization and Mapping Methods forResistive Neuromorphic Engines
1107	Hotspot Mitigation through Multi-Row Thermal-aware Re-Placement of Logic Cells based on High-Level Synthesis Scheduling
1109	Improving the Quality of Hardware Accelerators through automatic Behavioral Input Language Conversion in HLS
1111	Dynamic CNN Accelerator Supporting Efficient Filter Generator with Kernel Enhancement and Online Channel Pruning
1112	DVFSspy: Using Dynamic Voltage and Frequency Scaling As A Covert Channel for Multiple Procedures
1115	SynthNet: A High-throughput yet Energy-efficient Combinational Logic Neural Network
1119	Lamina: Low Overhead Wear Leveling for NVM with Bounded Tail
1127	A detailed-routability-driven deterministic parallel global router with soft capacity
1129	Large Forests and Where to "Partially" Fit Them
1130	XBM: A Crossbar Column-wise Binary Mask Learning Method for Efficient Multiple Task Adaption
1135	A Fast and Accurate Middle End of Line Parasitic Capacitance Extraction for MOSFET and FinFET Technologies Using Machine Learning
1137	Exploring ILP for VLIW architecture by Quantified Modeling and Dynamic Programming-based Instruction Scheduling
1138	HACScale: Hardware-Aware Compound Scaling for Resource-Efficient DNNs
1141	Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits
1143	Linear Feedback Shift Register Reseeding for Stochastic Circuit Repairing and Minimization
1147	This is SPATEM! A Spatial-Temporal Optimization Framework for Efficient Inference on ReRAM-based CNN Accelerator
1152	Reliable Memristive Neural Network Accelerators Based on Early Denoising and Sparsity Induction
1160	Heterogeneous Memory Architecture Accommodating Processing-In-Memory on SoC For AIoT Applications
1164	On the Viability of Decision Trees for Learning Models of Systems
1167	Design-for-Reliability and Probability-Based Fault Tolerance for Paper-Based Digital Microfluidic Biochips with Multiple Faults
1170	FPGA-Accelerated Maze Routing Kernel for VLSI Designs
1171	Efficient On-Device Incremental Learning by Weight Freezing
1174	A Heuristic Exploration to Retraining-free Weight Sharing for CNN Compression
1175	Toward Low-Bit Neural Network Training Accelerator by Dynamic Group Accumulation
1176	Voronoi Diagram Based Heterogeneous Circuit Layout Centerline Extraction for Mask Verification
1177	High-Correlation 3D Routability Estimation for Congestion-guided Global Routing
1178	Boosting ReRAM-based DNN by Row Activation Oversubscription
1185	Lithography Hotspot Detection via Heterogeneous Federated Learning with Local Adaptation
1188	Algorithm and Hardware Co-design for Reconfigurable CNN Accelerator
1193	Efficient Critical Paths Search Algorithm using Mergeable Heap
1194	Pearl: Towards Optimization of DNN-accelerators Via Closed-Form Analytical Representation

1196	NR-Router: Non-Regular Electrode Routing with Optimal Pin Selection for Electrowetting-on-Dielectric Chips
1197	An Accuracy Reconfigurable Vector Accelerator based on Approximate Logarithmic Multipliers
1202	WAL: A Novel Waveform Analysis Language for Advanced Design Understanding and Debugging
1209	Avatar: Reinforcing Fault Attack Countermeasures in EDA with Fault Transformations
1220	Anti-Piracy of Analog and Mixed-Signal Circuits in FD-SOI
1224	Signal-Integrity-Aware Interposer Bus Routing in 2.5D Heterogeneous Integration
1230	An Energy-Efficient Bit-Split-and-Combination Systolic Accelerator for NAS-Based Multi-Precision Convolution Neural Networks
1234	BSC: Block-based Stochastic Computing to Enable Accurate and Efficient TinyML
1236	Optimal Loop Tiling for Minimizing Write Operations on NVMs with Complete Memory Latency Hiding
1237	A Versatile Mapping Approach for Technology Mapping and Graph Optimization
1238	Fast Electromigration Stress Analysis Considering Spatial Joule Heating Effects
1244	Data Leakage through Self-Terminated Write Schemes in Memristive Caches
1246	HiKonv: High Throughput Quantized Convolution With Novel Bit-wise Management And Computation
1248	Boolean Rewriting Strikes Back: Reconvergence-Driven Windowing Meets Resynthesis
1271	CGRA Mapping Using Zero-Suppressed Binary Decision Diagrams
1280	Multi-Precision Deep Neural Network Acceleration on FPGAs
1281	EdgeⁿAI: Distributed Inference with Local Edge Devices and Minimum Latency
1284	Time-Triggered Scheduling for Time-Sensitive Networking with Preemption
1289	Energy Harvesting Aware Multi-hop Routing Policy in Distributed IoT System Based on Multi-agent Reinforcement Learning
1290	AdaSens: Adaptive Environment Monitoring by Coordinating Intermittently-Powered Sensors
1291	Delay Optimization of Combinational Logic by And-Or Path Restructuring
1294	Net Separation-Oriented Printed Circuit Board Placement via Margin Maximization
1295	Streaming Accuracy: Characterizing Early Termination in Stochastic Computing
1298	STREAM: Towards READ-based In-Memory Computing for Streaming based Data Processing
1303	Transient Adjoint DAE Sensitivities: a Complete, Rigorous, and Numerically Accurate Formulation
1308	HybridGP: Global Placement for Hybrid-Row-Height Designs
1311	Acronymn*: An Open-Source Analytical Placer for Large Scale Heterogeneous FPGAs using Deep-Learning Toolkit
1320	Boosting the Search Performance of B+-tree with Sentinels for Non-volatile Memory