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A 5.2GHz RFID Chip Contactlessly Mountable on FPC at Any 90-Degree Rotation and Face Orientation

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Systems Design Lab

Outline

- Introduction
- Proposed method
  - Bonding-less structure
  - High frequency implementation
- Experimental results
- Conclusion

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- **Introduction**
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  - High frequency implementation
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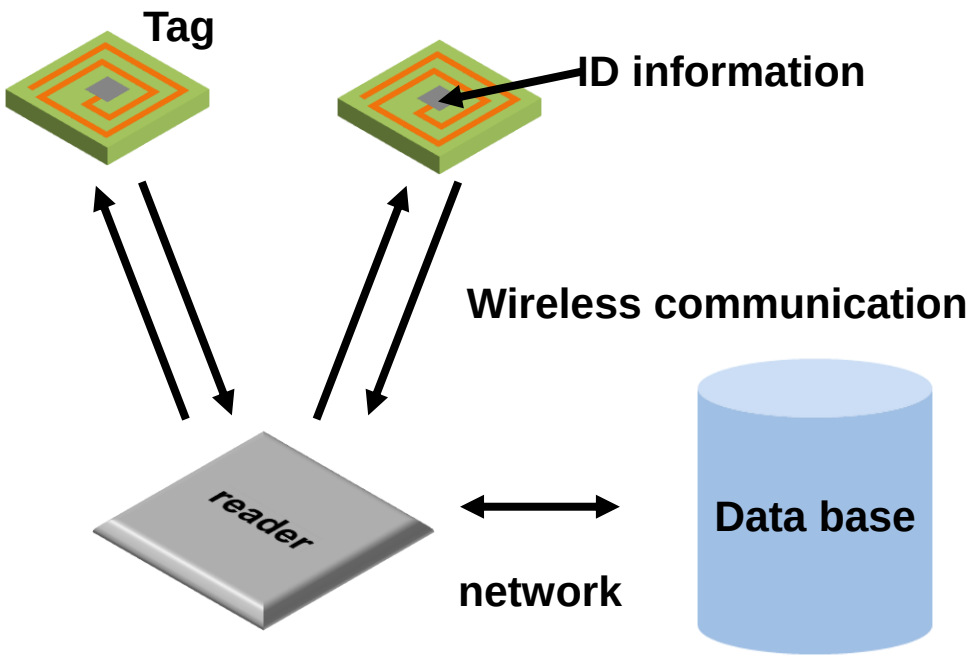
Introduction

- RFID=Radio Frequency Identification
- The ID information on tags are communicated to a nearby reader, and reader accesses database via Internet

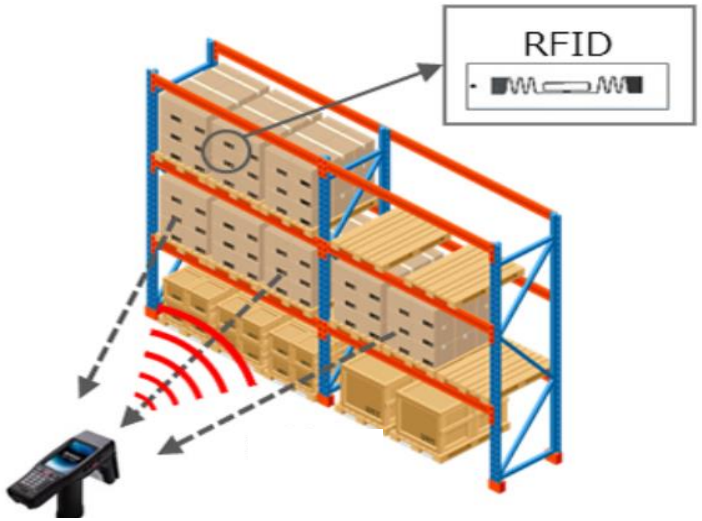


RFID system

Application

- RFID is applied to unmanned cash register and inventory management
- To fulfill RFID potential, tags need to be low cost

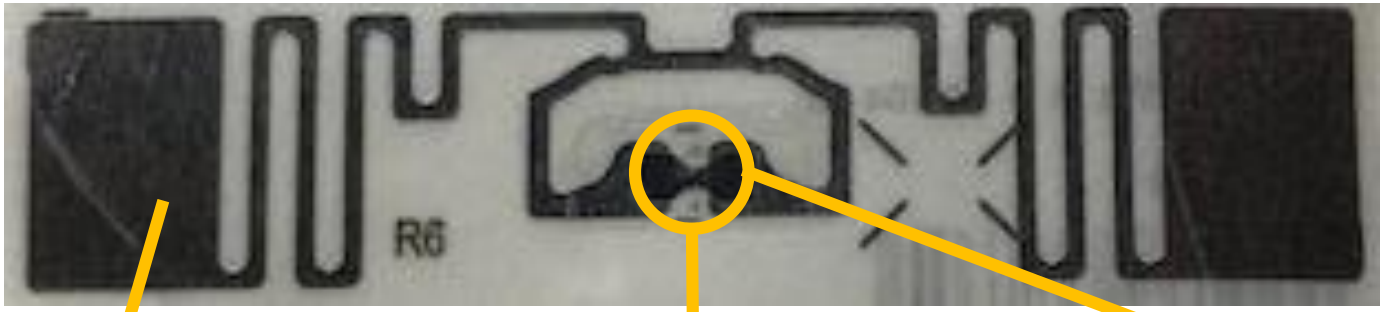
Unmanned cash register



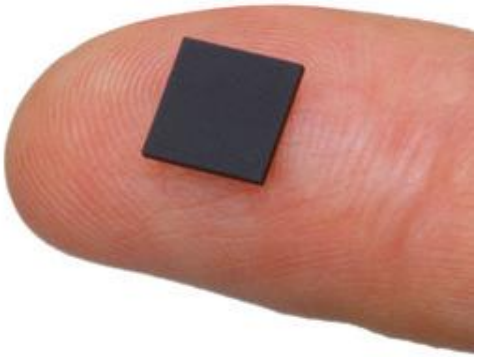
Inventory control

RFID tag manufacturing cost

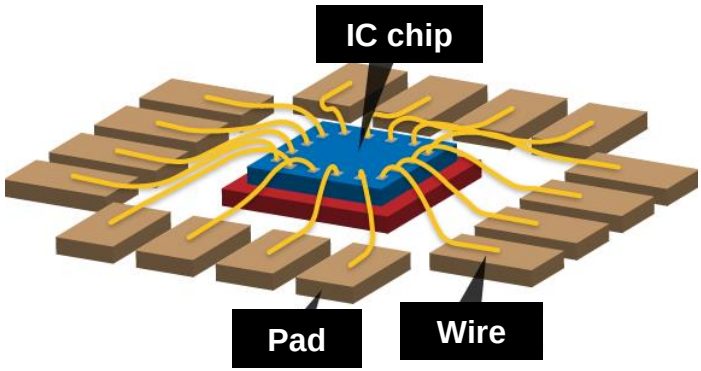
- **Antenna cost, IC-chip cost, Bonding cost**



Tag antenna



IC chip



Bonding

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- **Proposed method**
  - **Bonding-less structure**
  - **High frequency implementation**
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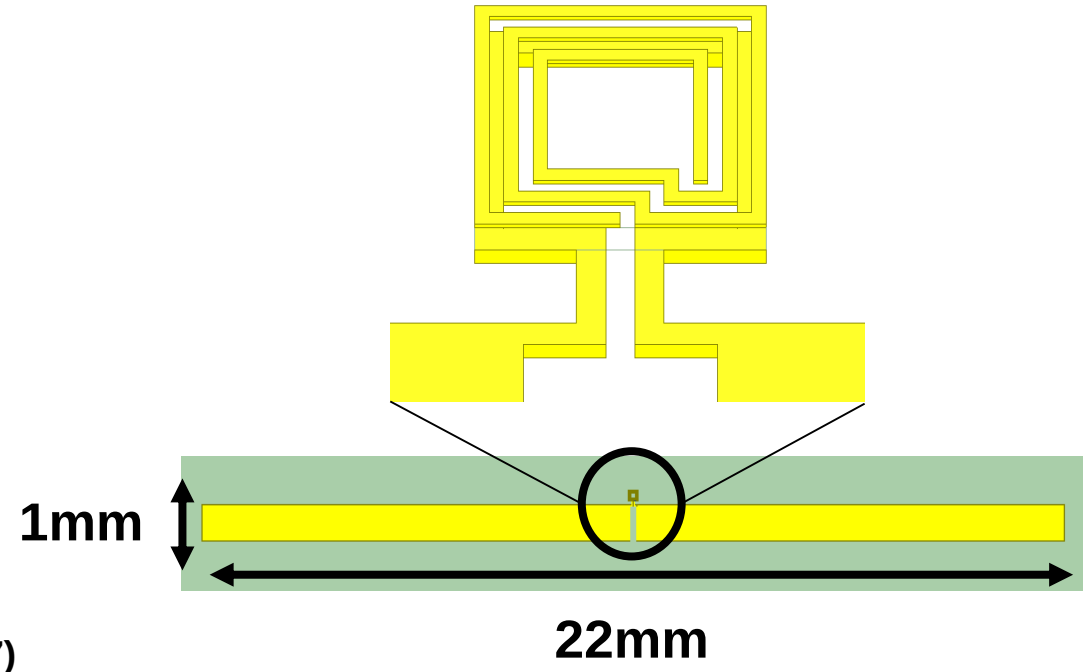
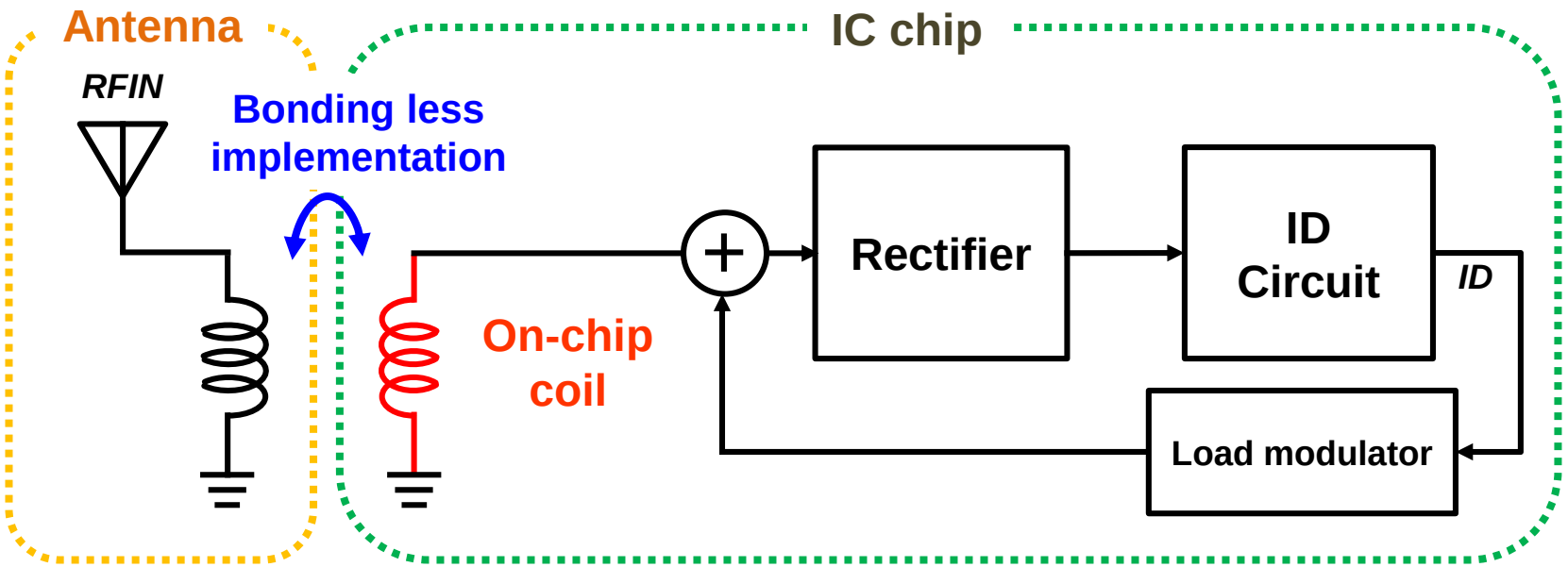
Proposed method

- A bonding-less 5-GHz RFID module
- Wireless connection between chip and antenna
  - Significant reduction in bonding costs
- High frequency
  - a 95% downsized antenna



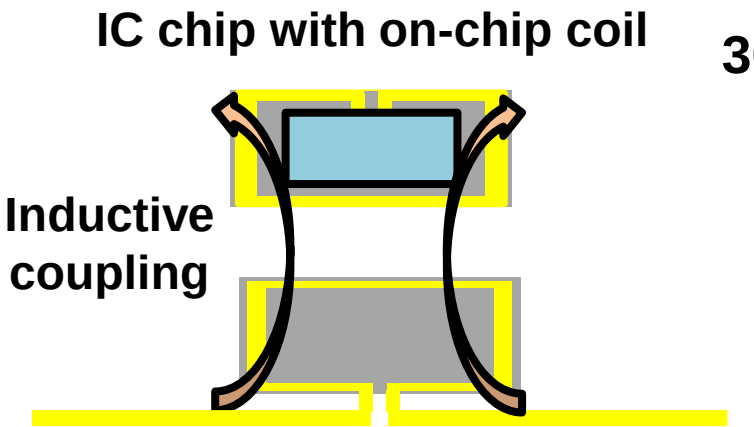
Block diagram of the module

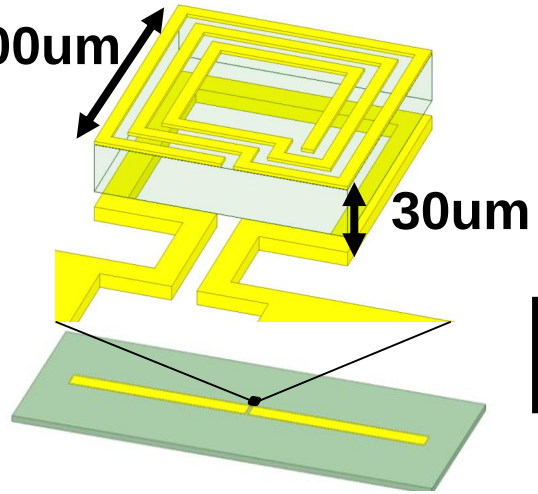
- The antenna and the IC chip communicate wirelessly by inductive coupling
- The IC chip consists of the on-chip coil, the rectifier, the ID circuit, and the load modulator

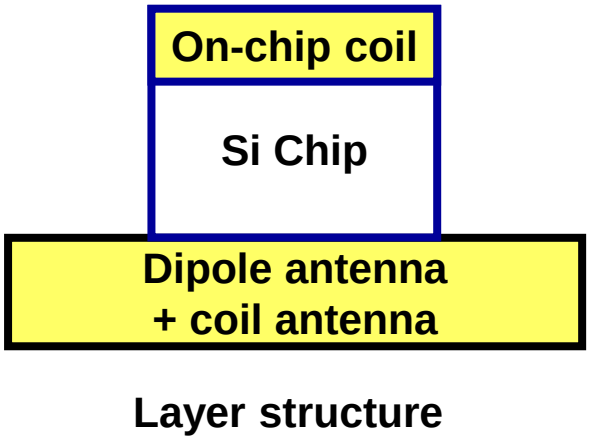


Bonding-less structure

- The antenna is made up of two components
  - a conventional dipole antenna
  - a coupling structure to provide inductive coupling
- Coil diameter: 300um
- Distance between coils: 30um

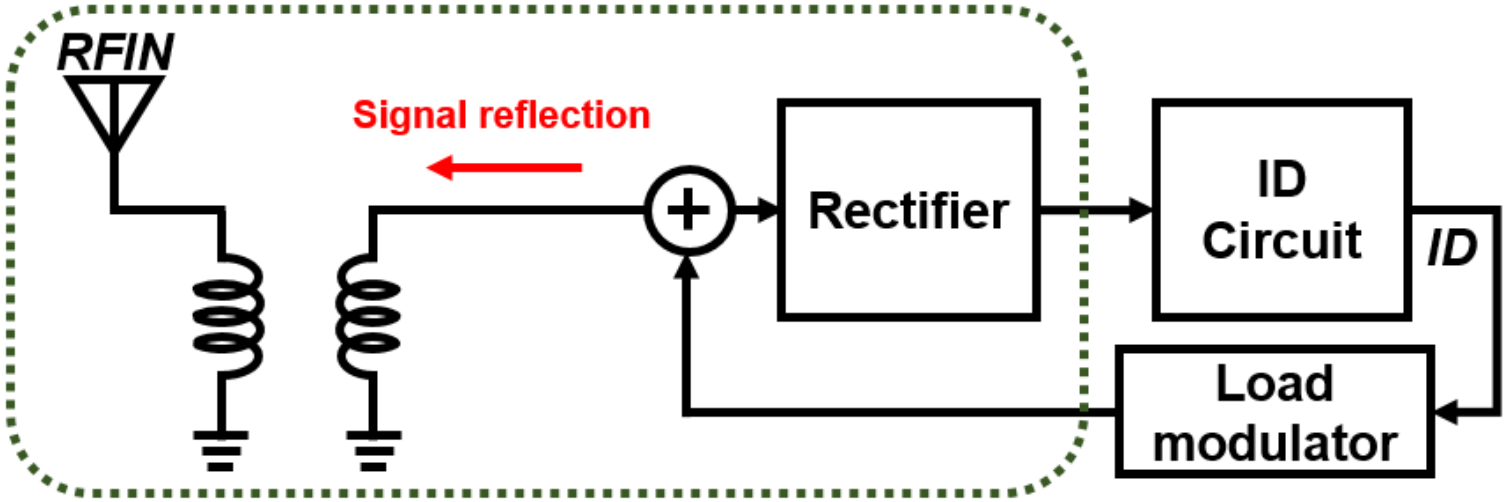






High frequency implementation

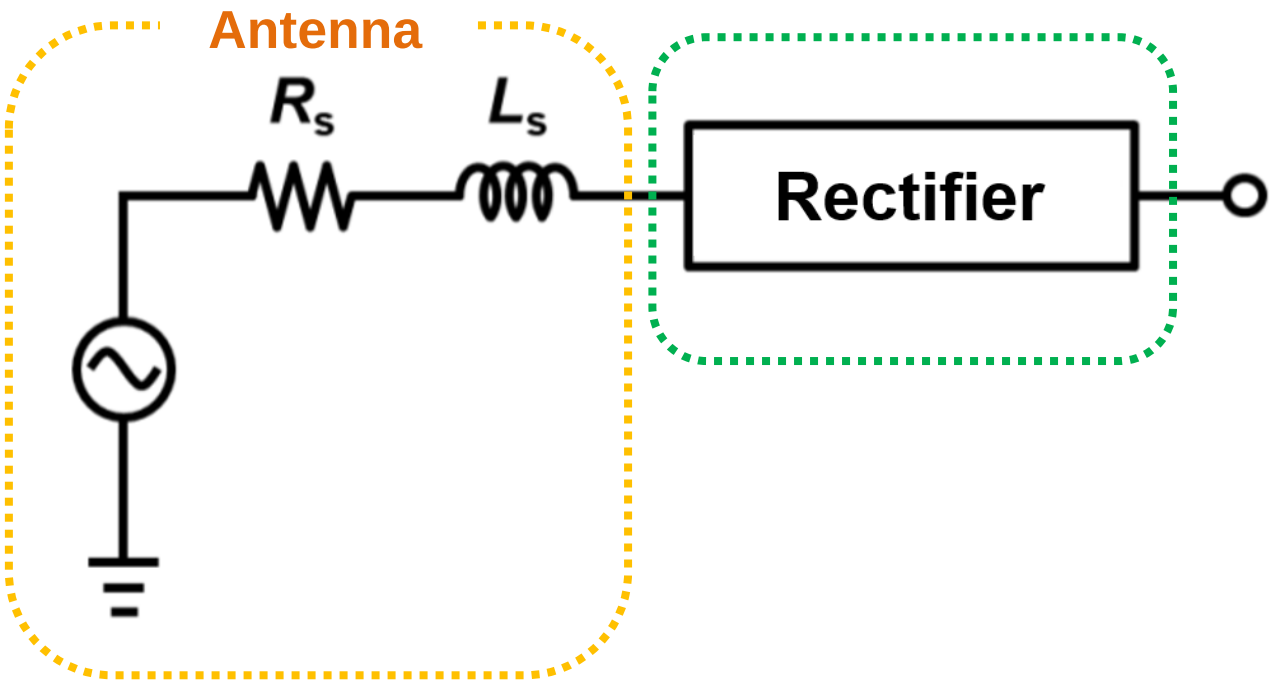
- **Reduced received power**
  - **An increase of signal reflection**
- **Impedance matching between antenna and rectifier is required**
  - **The input impedance of the rectifier being nonlinear and dependent on the input voltage and output current**



Block diagram of the module

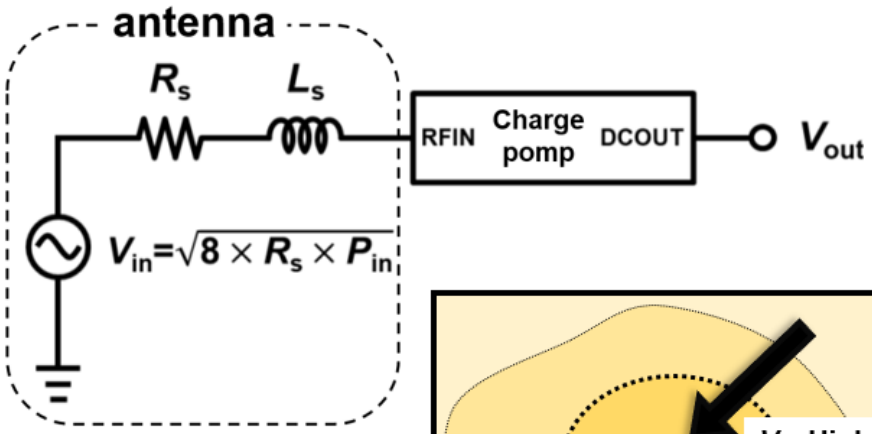
Design methodology for impedance matching

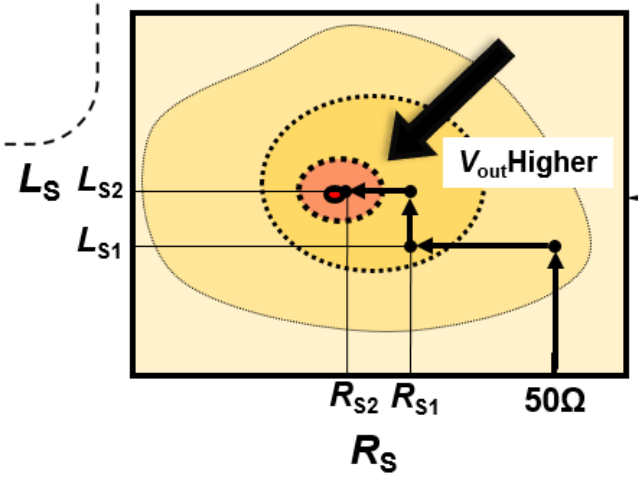
- The input impedance of the rectifier design
- Antenna design
  - Impedance matching L_S
  - Impedance matching R_S

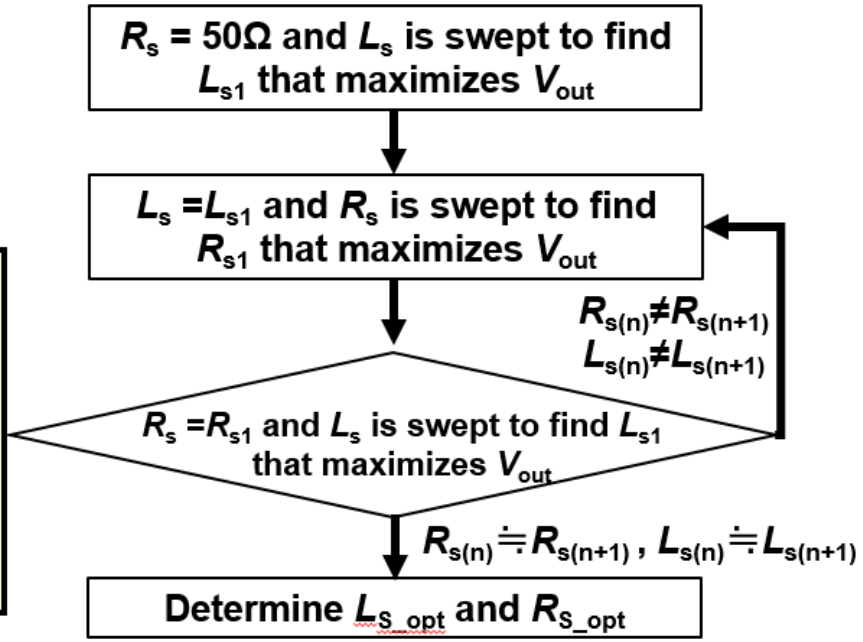


The input impedance design

- The sweeping of R_s and L_s is repeated to obtain R_{s_opt} and L_{s_opt} that maximize V_{out} at 5.2GHz
- R_{s_opt} =4.5Ω, L_{s_opt} =4.6nH



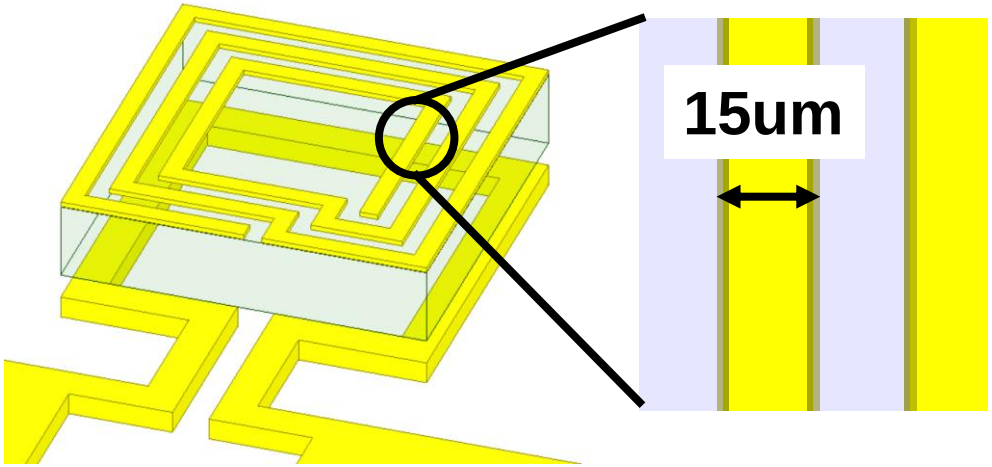


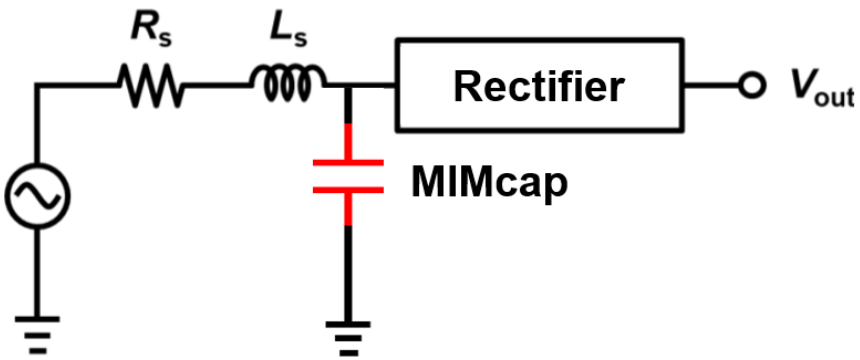


P_{in} : The received power(set to -10dBm) V_{out} : The out put Voltage

Impedance matching L_S

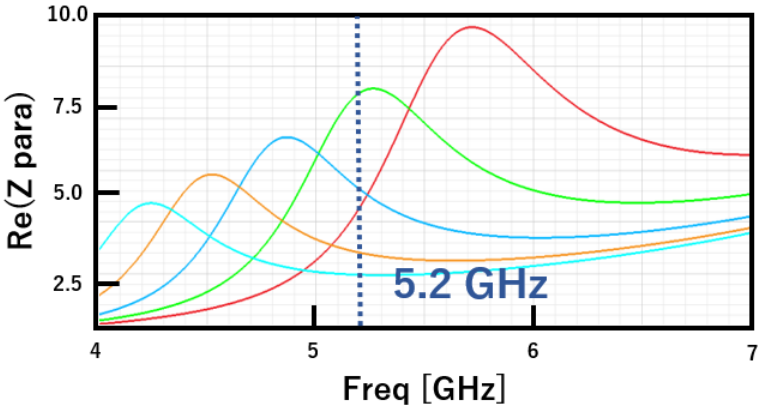
- Design the on-chip coil for maximum inductance
  - Increased number of turns (N = 3)
  - Metal width optimization (15um)
- A matching circuit using a MIM capacitor is inserted to improve impedance matching

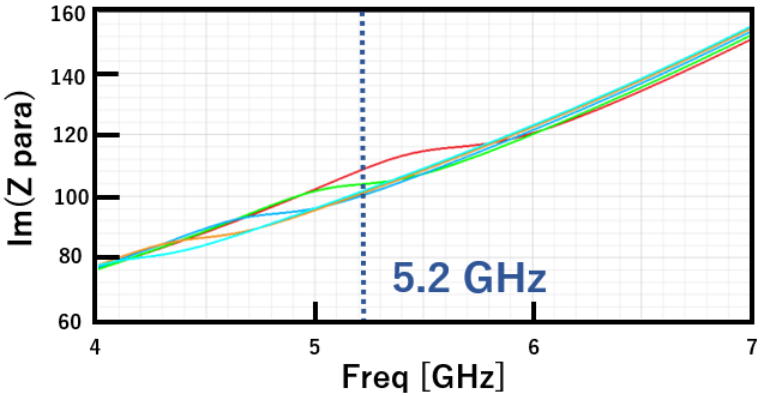


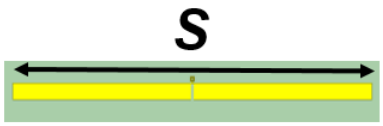


Impedance matching R_S

- The gain and imaginary part are almost constant
- The real part varies significantly
  - ◆It is possible to design R_{s_opt} while maintaining the gain and the antenna inductance at their desired values





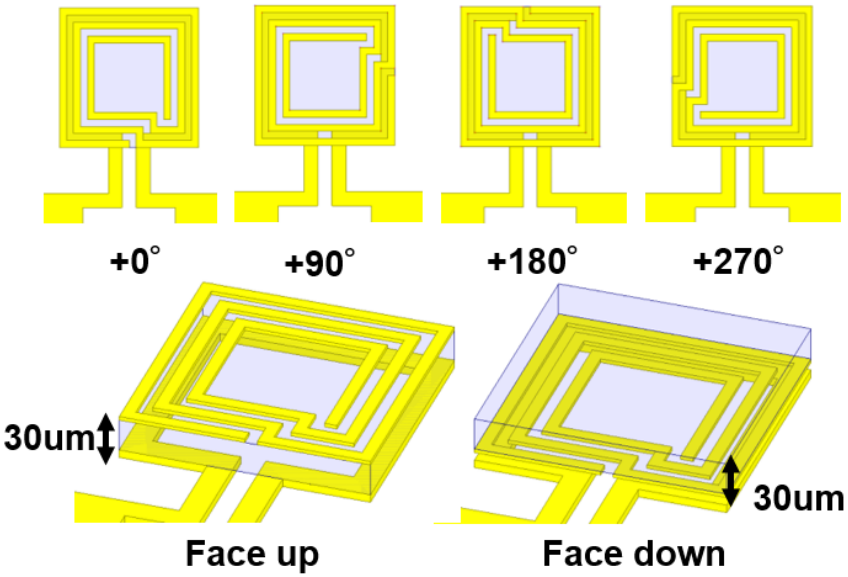


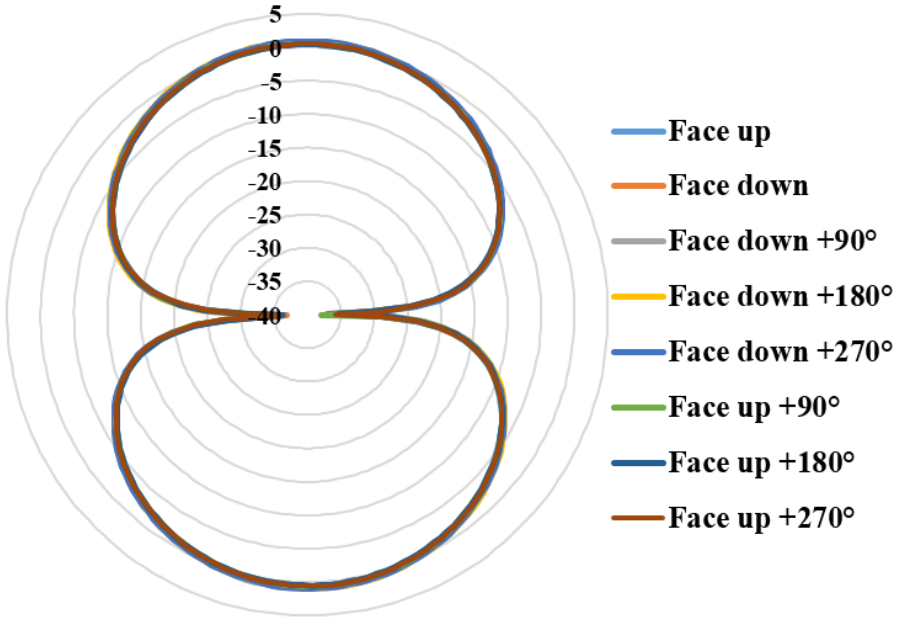
S	Gain
S=0.312λ	0.8
S=0.347λ	1.2
S=0.382λ	1.0
S=0.417λ	0.8
S=0.452λ	0.6

λ : Wave length

Antenna gain under 8 conditions

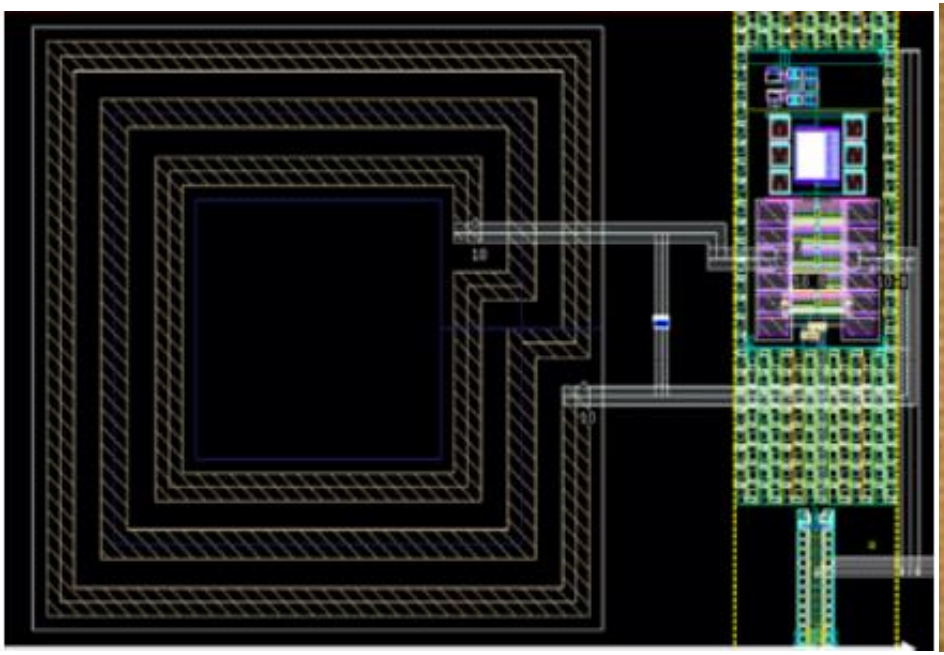
- The performance of the antenna is almost the same within 0.5 dB deviation
- The chip can be mounted on the FPC using any of these 8 geometric variations



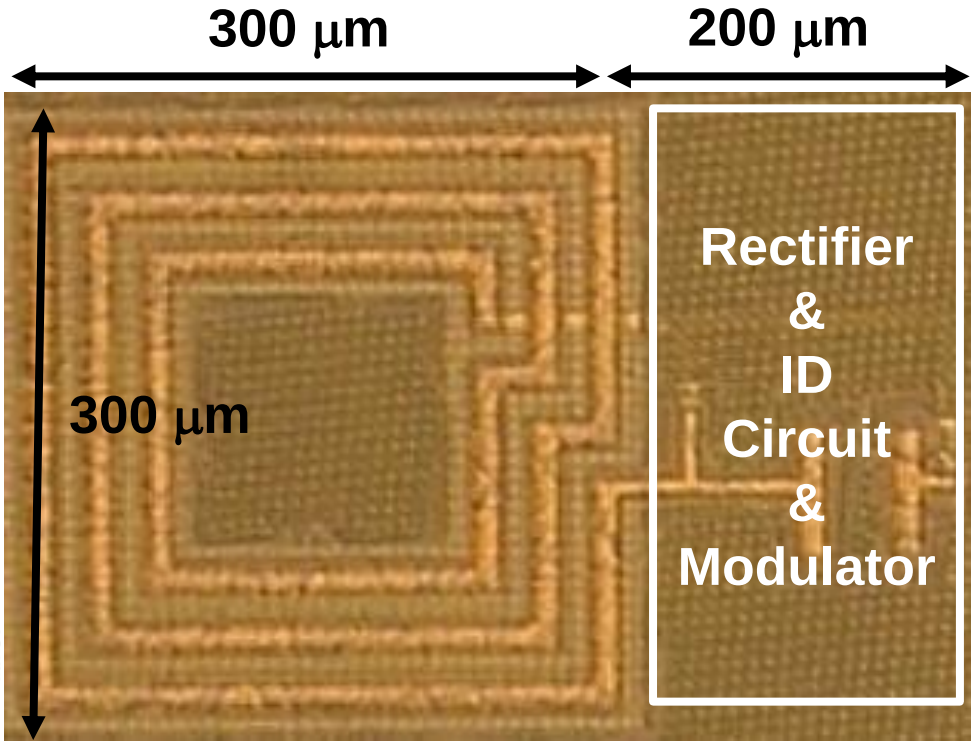


Tag chip photo

- The chip fabricated in 180nm CMOS is 300um x 500um



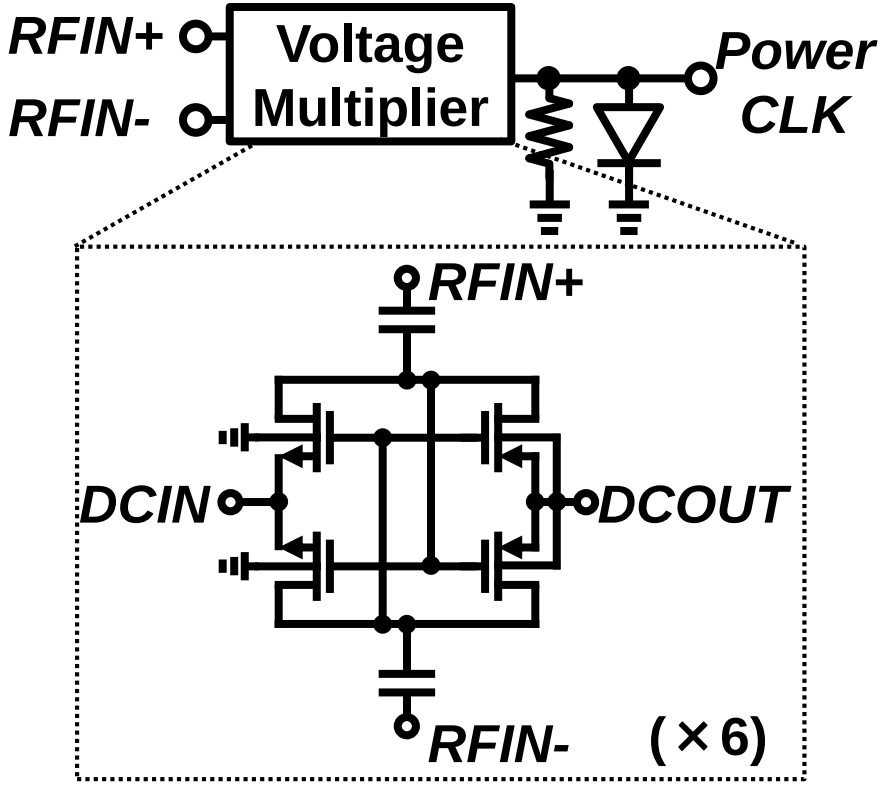
The chip layout

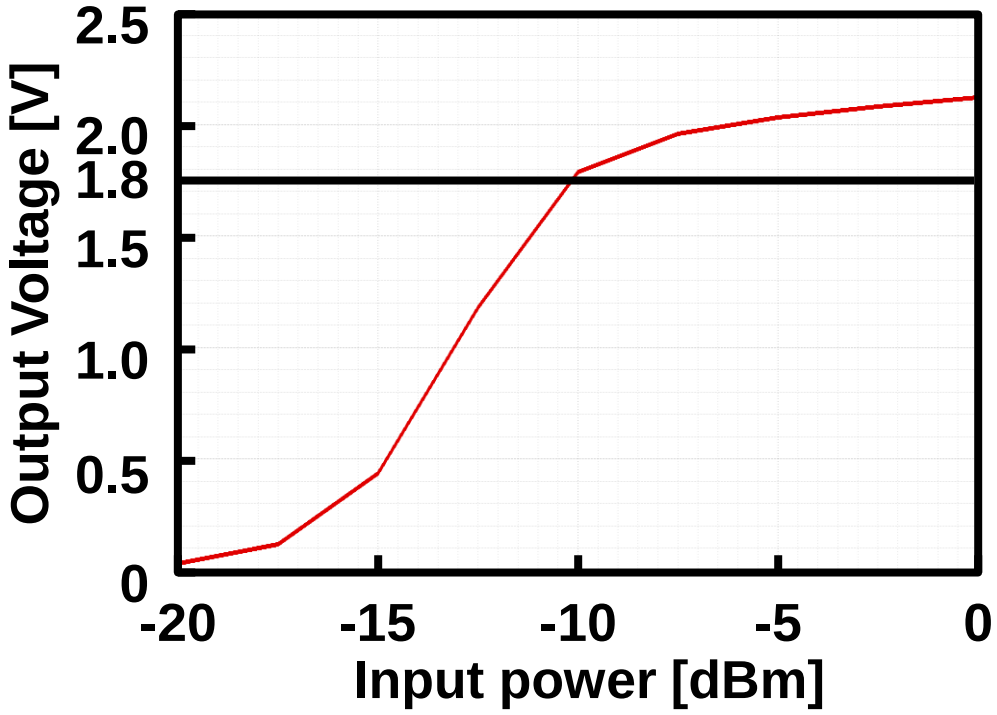


The chip photo

The CMOS rectifier[1]

- 6-stage CMOS cross-couple charge pump and resistance load

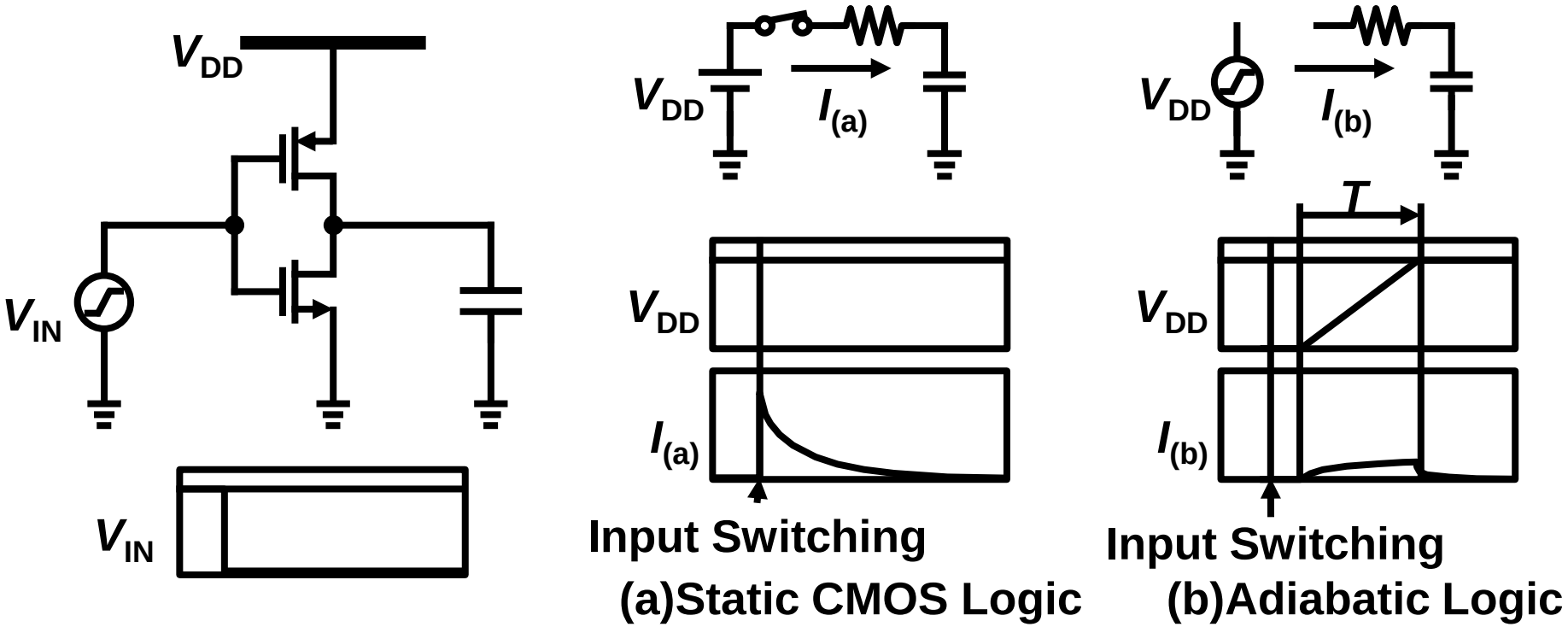




[1] : M. Stoopman et al., *IEEE JSSC*, March 2014, pp. 622–634.

ID Circuit using adiabatic Logic[2]

- **Charging/Discharging current is reduced by varying supply voltage**
  - **Consume lower power**
  - **Driven by power clock**

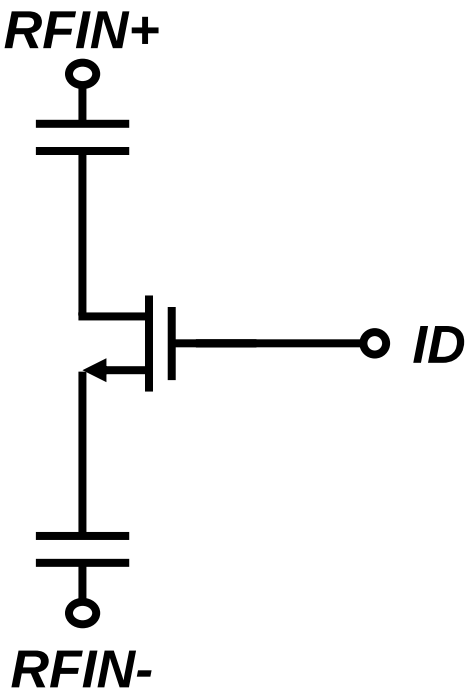


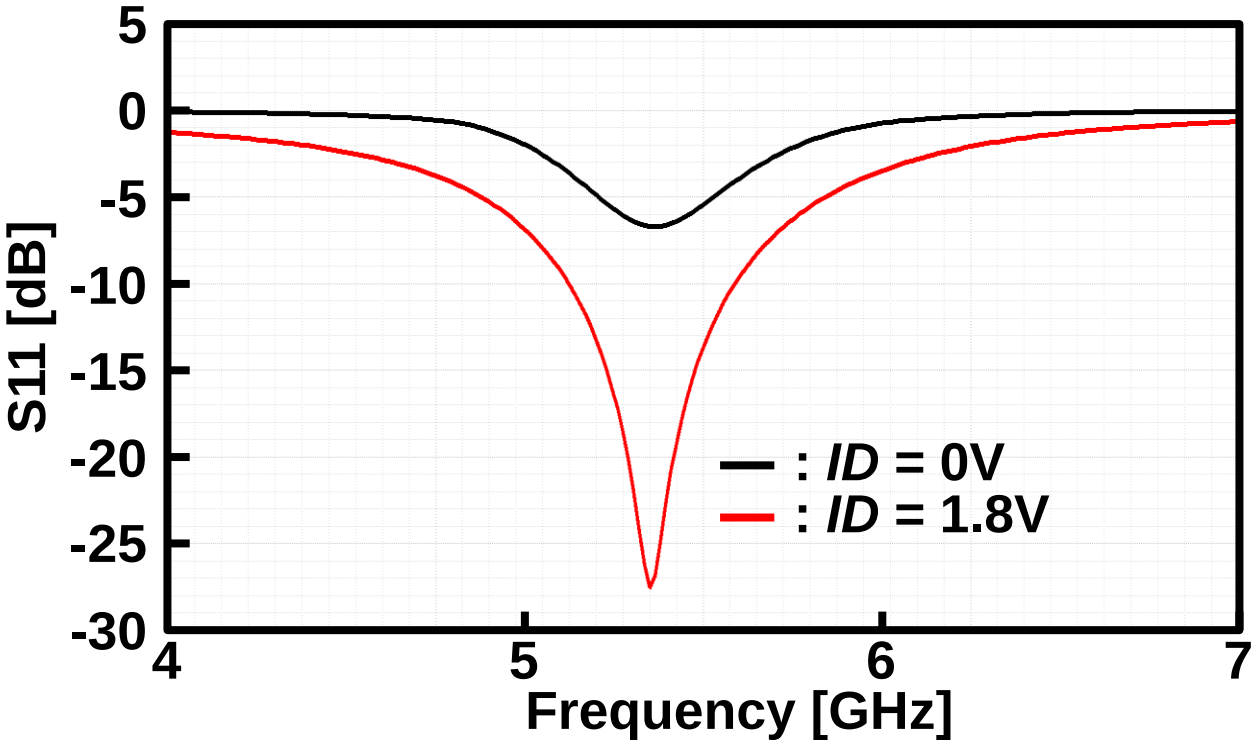
(a)Static CMOS Logic (b)Adiabatic Logic

[2]: J. Hu et al., MWSCAS, 2005, pp.1398-1401.

Modulator

- **Depends on the modulation method**
  - **Load modulation circuit**





Reflection characteristics of antenna and internal circuit

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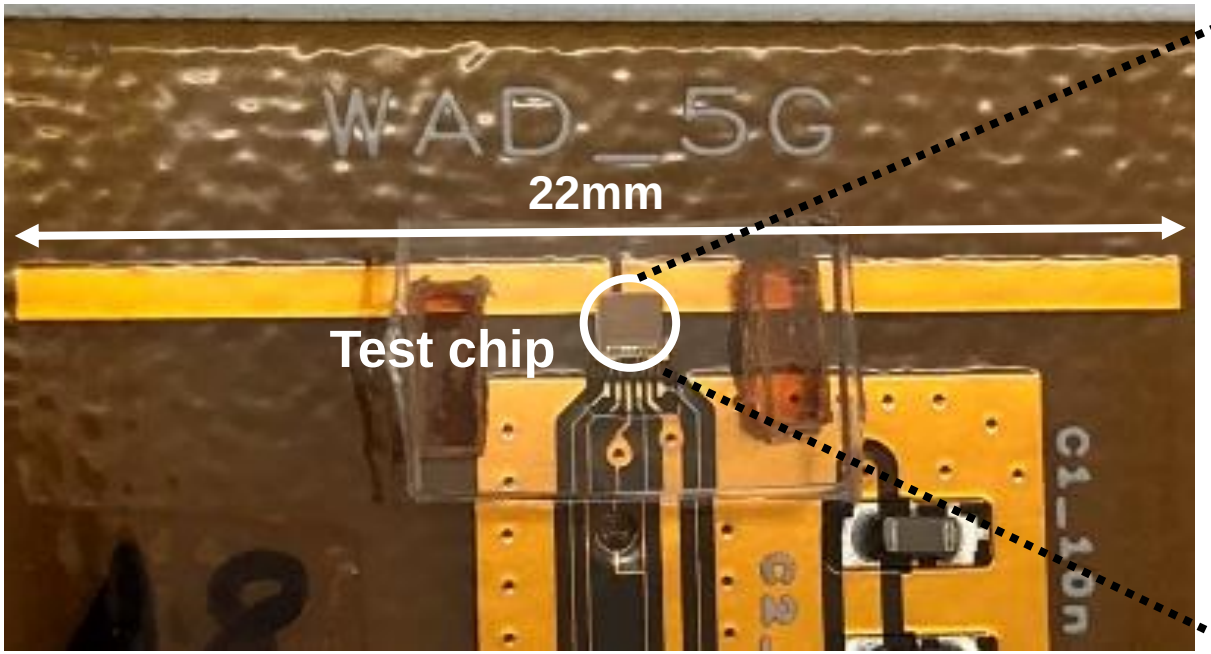
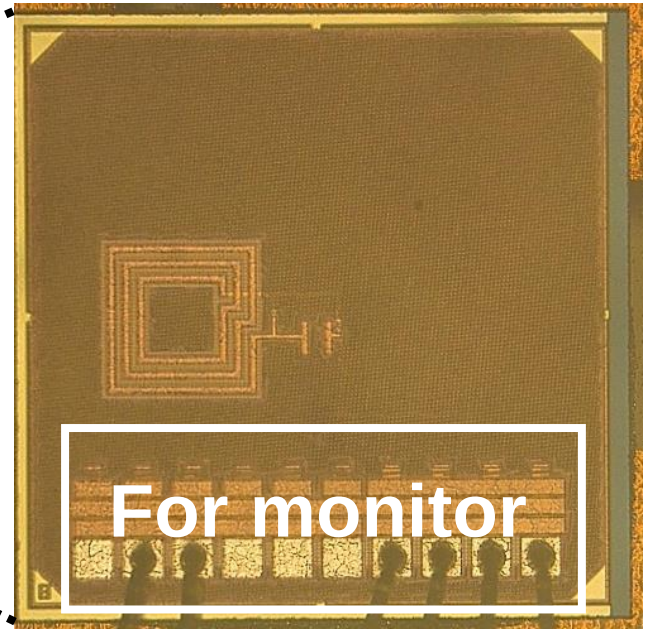
The chip implementation on FPC

- The antenna was made using FPC
- Antenna size : 22mm x 1mm



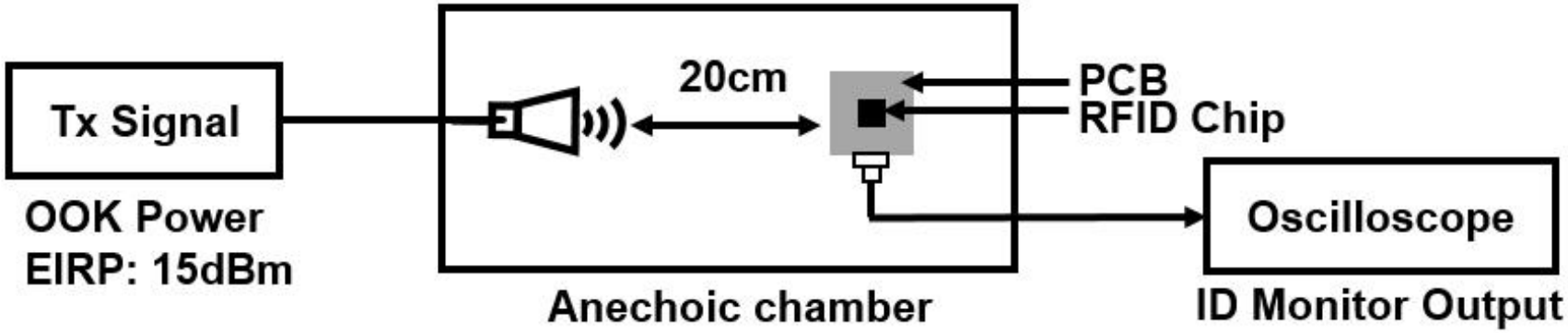
Photograph of proposed RFID module

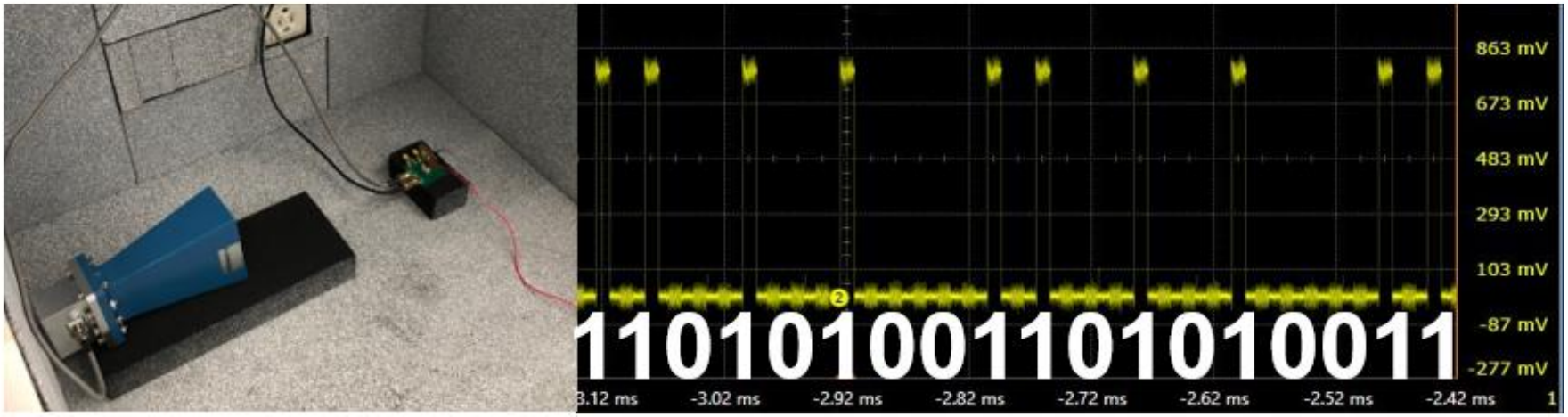


Test chip

Experimental results

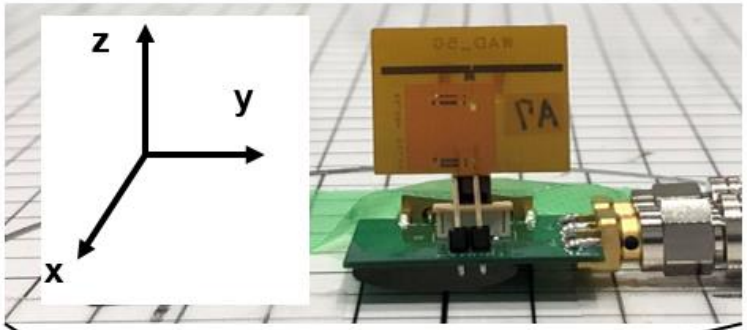
- **The RFID module successfully worked at 20cm from a reader whose output power is 15dBm**

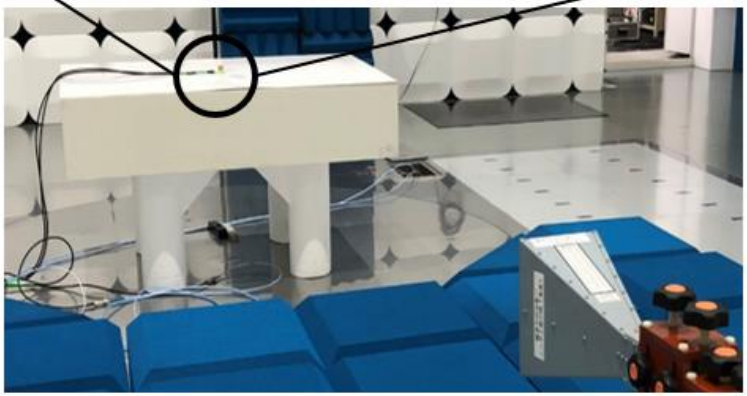


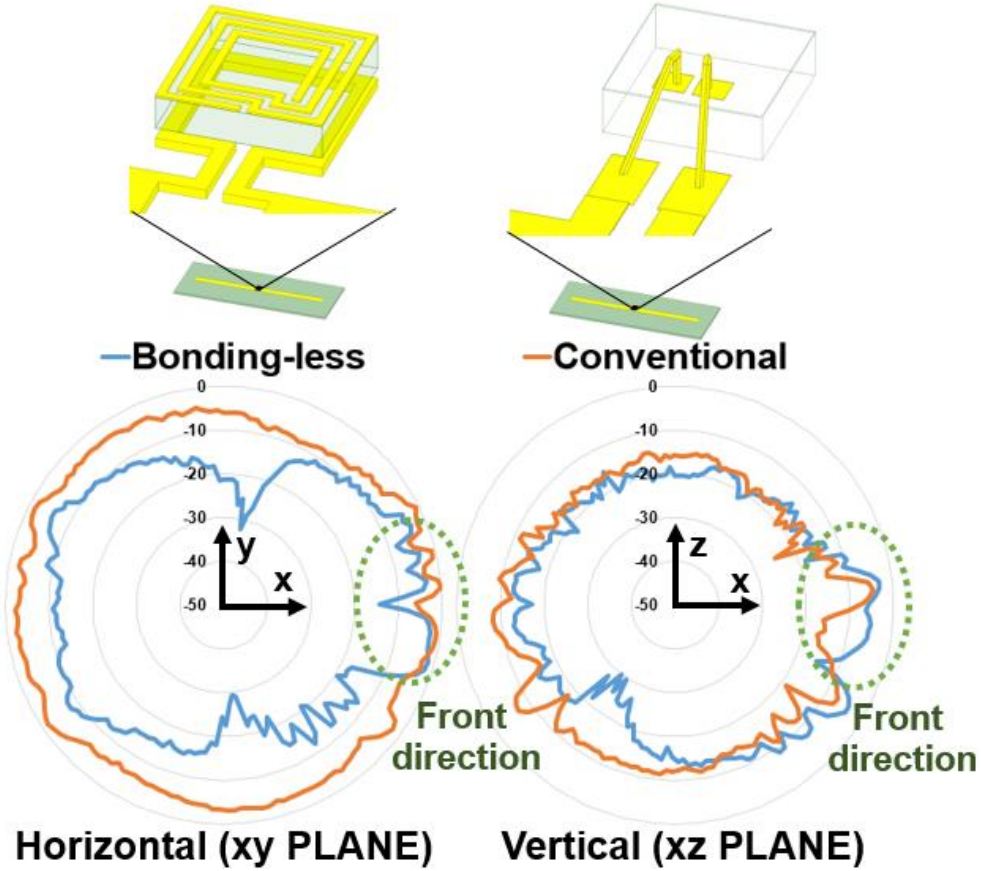


Measured antenna gain

- **The gain of the antenna was increased to almost the same as that of the dipole antenna in the front direction**



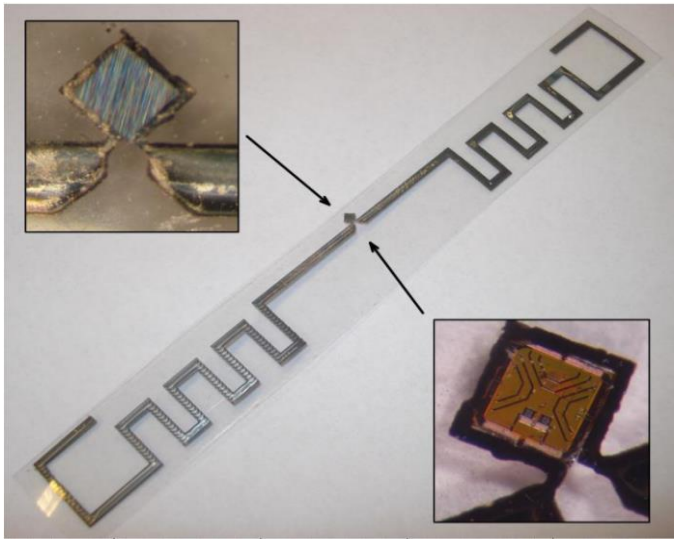




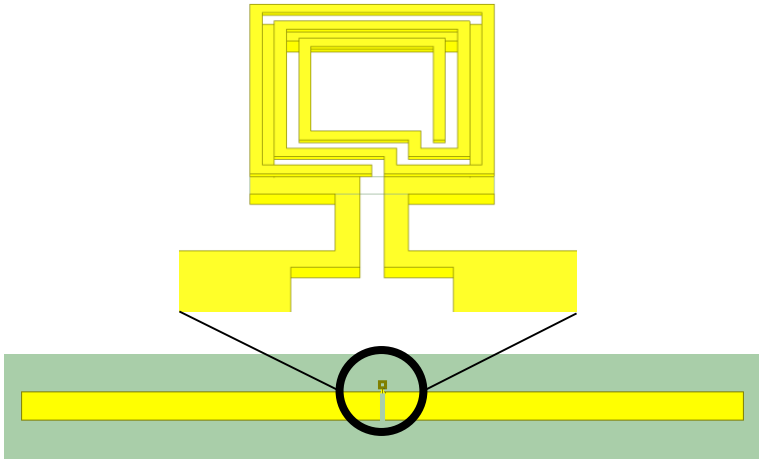
Performance Comparison

Reference	[3]	This work
Frequency	UHF	5.2 GHz
Antenna size (ratio)	1000mm^2 (22.7)	22mm^2 (1)
Tag chip size ratio	6.6	1
Technology	0.13 um CMOS	0.18 um CMOS
EIRP	36 dBm	15 dBm
Working distance	210 cm	20 cm
FoM	10.85	13.83

$$\text{FoM} = \frac{\text{Range}}{\frac{\sqrt{\text{Area}}}{\lambda} \times \sqrt{\text{EIRP}}}$$



The UHF bonding-less module [3]



This work(5GHz bonding-less)

[3] Walther Pachler, et al., IEEE EUCAP 2013

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  - ◆Wireless connection between chip and antenna
    - Significant reduction in bonding costs
  - ◆High frequency
    - a 95% downsized antenna
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