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Fast Variation-aware Circuit Sizing Approach for Analog Design with ML-Assisted Evolutionary Algorithm

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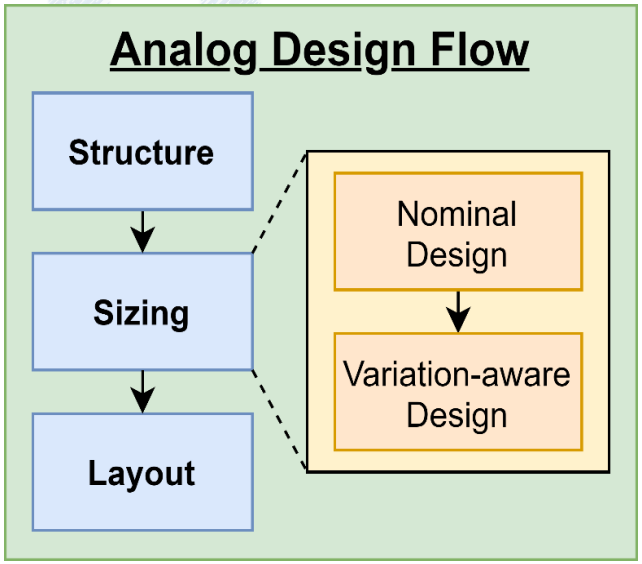
Outline

- Introduction
- Proposed Circuit Sizing Methodology
- Experimental Results
- Conclusion

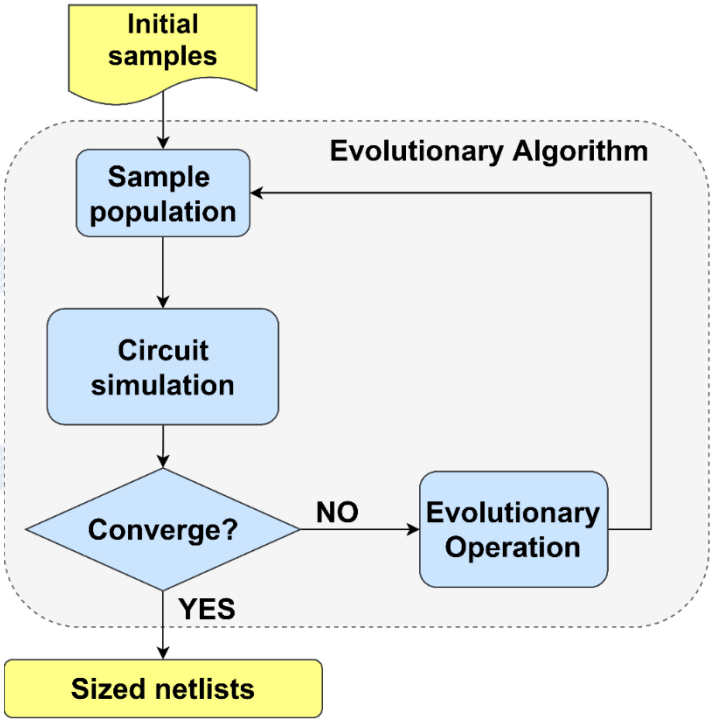
Analog Circuit Sizing Challenges

- Manually sizing analog circuit is a complicated task
  - Non-linear characteristics
  - Sensitive to process variation
  - Suffer from expensive simulation
- Two steps in analog circuit sizing
  - Optimize the nominal performance
  - Optimize the parametric yield under process variation
- Automatic circuit sizing is necessary



Traditional Simulation-based Sizing

- Simulation-based sizing
  - Simulated annealing (SA)
  - Evolutionary algorithm (EA)
- Accurate but slow
  - Require many iterations to converge
  - Each iteration requires expensive simulations
- ML-assisted analog sizing
  - BagNet[1]
  - AutoCkt[2]
  - ESSAB[3]
  - Previous works tried to replace simulator
- Most of them do not consider process variation

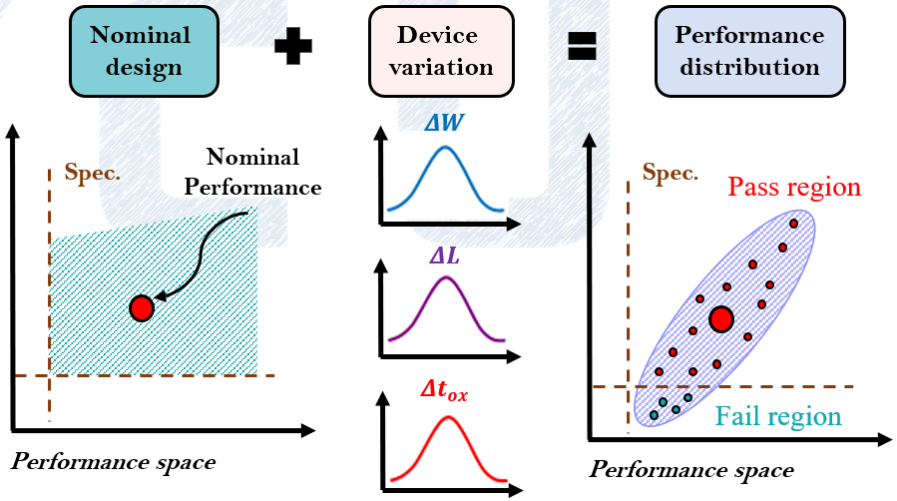


[1] K. Hakhamaneshi, et. , "BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks," ICCAD, pp. 1-8, 2019.
[2] K. Settaluri, et., "AutoCkt: Deep Reinforcement Learning of Analog Circuit Designs," DATE, pp. 490-495, 2020.
[3] A. Budak, et., "An Efficient Analog Circuit Sizing Method Based on Machine Learning-Assisted Global Optimization," in IEEE TCAD, Early Access.

Synthesis with Variations

- In advanced technology, device variations become the major factor limiting circuit performance
  - Variations are often not considered in traditional sizing algorithms
- Effects of process variations may change
  - Transistor width (W)
  - Channel length (L)
  - Oxide thickness (t_{ox})
  - …

  →Circuit performance



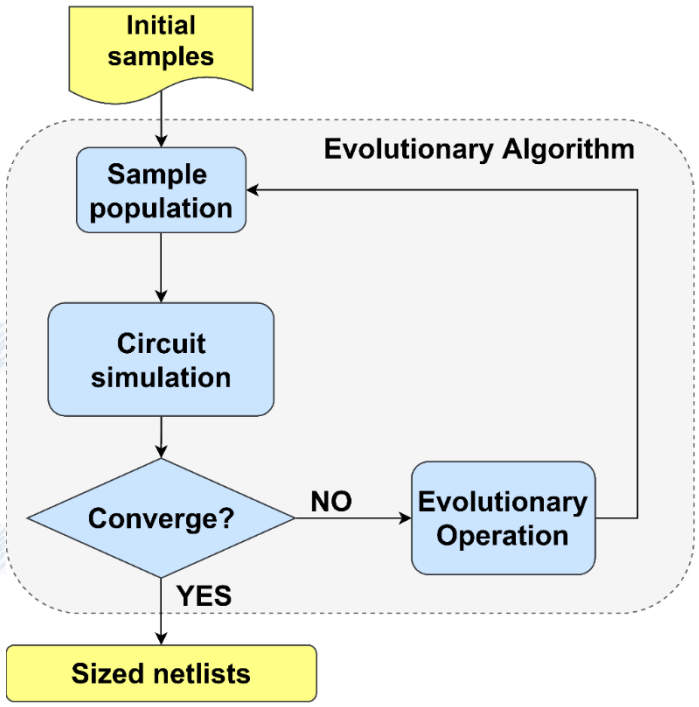
- The feasible nominal circuit may have a serious yield loss

[4] Y. Chen, W. Wu, C. J. Liu, and J. C. Li, "Simultaneous Optimization of Analog Circuits With Reliability and Variability for Applications on Flexible Electronics," in IEEE TCAD, vol. 33, no. 1, pp. 24-35, Jan. 2014.

ORDE

- Variation-aware analog sizing
  - ORDE[5]
    - Reduce Monte-Carlo samples by optimal computing budget allocation

→Not improve the converge capability



Many useless candidates are generated

[5] B. Liu et., "Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques," in IEEE TCAD, vol. 30, no. 6, pp. 793-805, June 2011.

Contributions

- In this work
  - Machine learning-assisted evolutionary algorithm
    - Pruning the required simulation amount
    - Enhancing the convergence speed of the search engine
  - Fast yield evaluation without using Monte Carlo analysis
    - Force model
    - Reduce the computational cost of yield evaluation
  - Aid designer to optimize design with robustness

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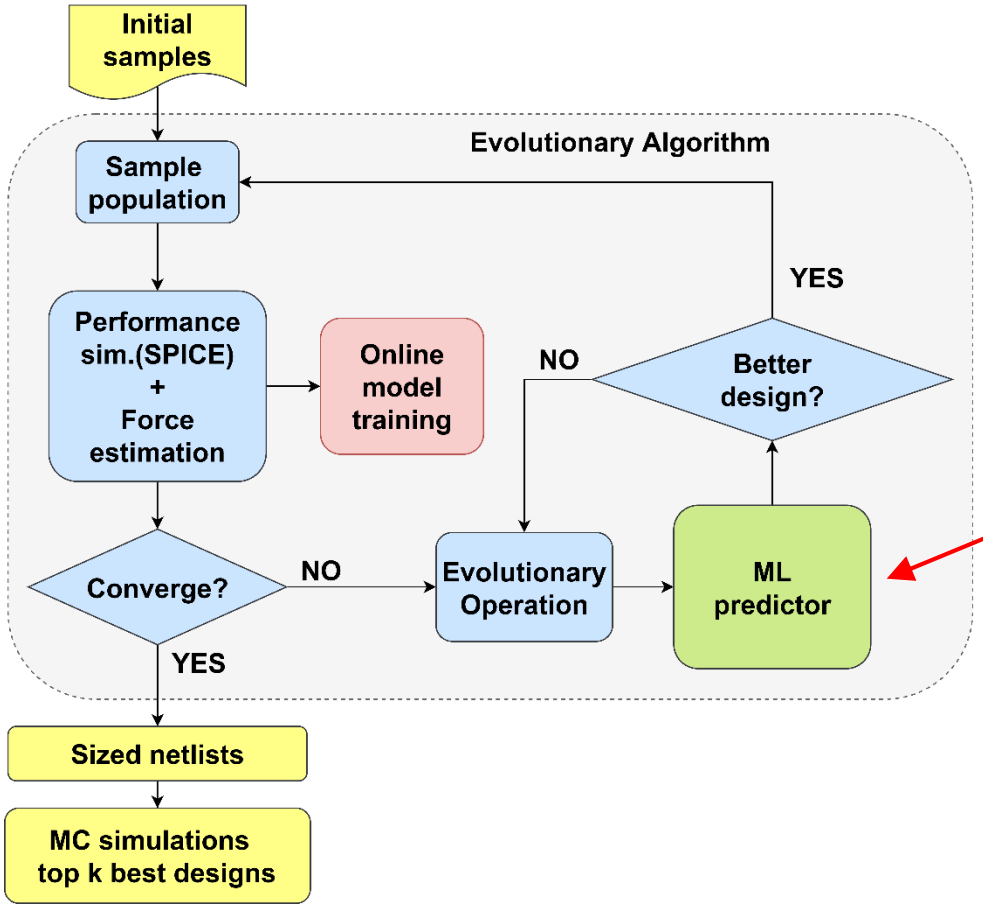
ML-assisted Analog Sizing

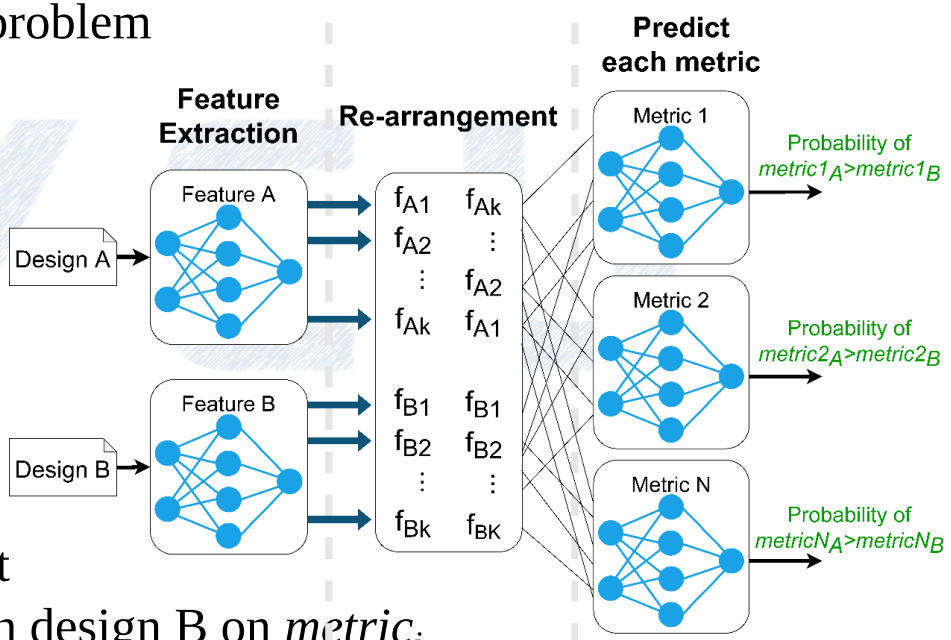
- ML model helps to screen out useless simulations



Predictor chooses design samples that are very likely to have better performance

Prediction Model

- Predicting the exact performance is difficult and unnecessary
  - Predicting a sample is "better" or "worse" is easier[4]
    - Binary classification problem

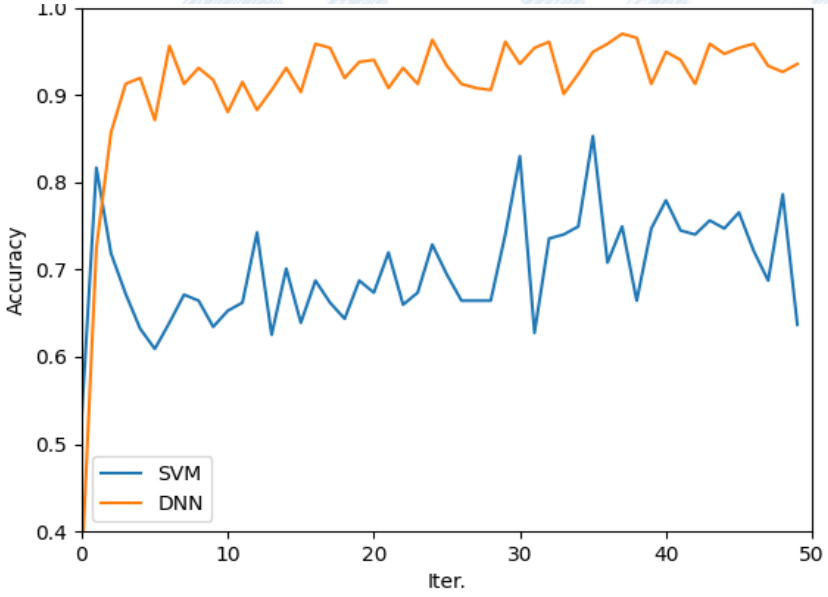


- Prediction model
  - Input
    - Two circuit designs
  - Output
    - The probability of that design A is better than design B on $metric_i$
  - Online model training will continuously improve the accuracy

[4] K. Hakhamaneshi, N. Werblun, P. Abbeel, and V. Stojanović, "BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks," ICCAD, pp. 1-8, 2019.

Model Comparison

- The proposed model is similar to a binary classification
  - Often solved by support vector machine (SVM) model
- From the experiment, DNN is always better than SVM
  - Relationship of analog circuits is too complicated for SVM
  - Select DNN as our prediction model



- Sizing same circuit with 50 iterations by SVM and DNN
- Compare model accuracy with real simulation data

Variation-aware Sizing

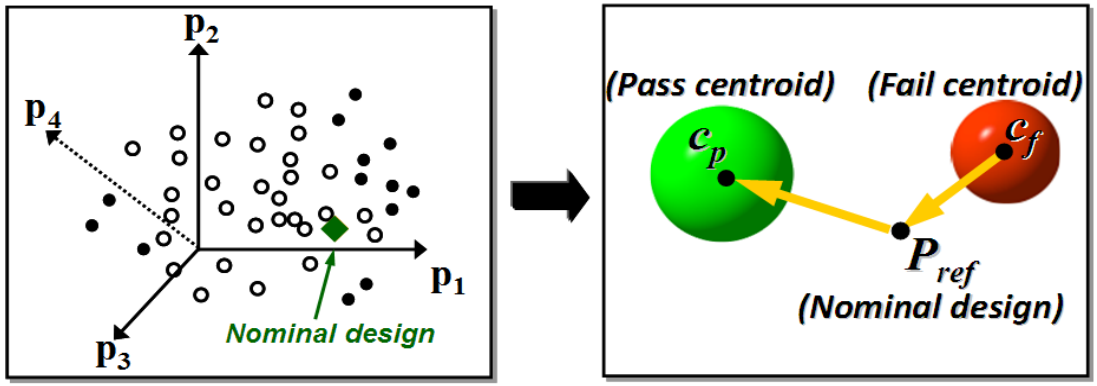
- Including process variations consideration, the robustness of solution is guaranteed

- Difficulty comes from the way to obtain design yield
  - Monte Carlo (MC) analysis is the most common approach
    - Huge amount of simulations
  - Few MC analyses are required for each sizing iteration
    - Extremely time-consuming
    - Infeasible for large circuit

- Require an efficient approach to evaluate the design yield
  - Force-directed model

Force-directed Model[9]

- Imagine the Pass/Fail samples are in an energy system
  - Nominal design is the reference point (P_{ref})
- Determine the new nominal point with better yield
  - Far from the Fail group (repulsion)
  - Close to the Pass group (attraction)



Performance level

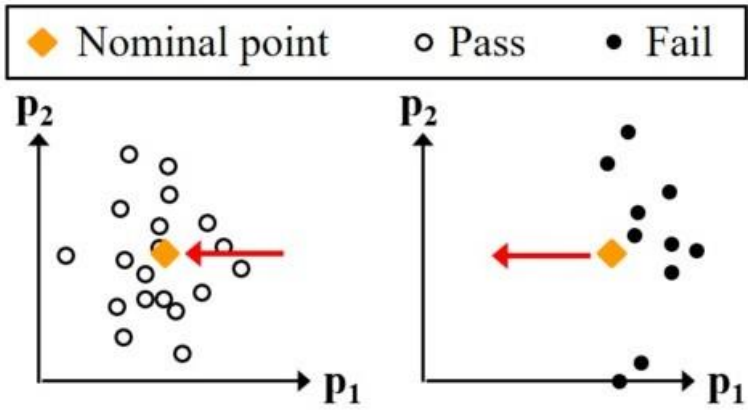
[9] C. Kuo, Y. Chen, I. Tsai, L. Chan, and C. J. Liu, "Behavior-level yield enhancement approach for large-scaled analog circuits," Design Automation Conference, pp. 903-908, 2010.

Yield Estimation with Force Model

- Use the magnitude of the resultant force as rough yield estimation
  - Replace the expensive MC simulation

$$F_{cd} = \sum_{p \in PASS} \vec{D}_p + \sum_{f \in FAIL} \vec{D}_f$$

$$\vec{D}_p = \sum_i (c_i^{cd} - c_i^p)/c_i^* \qquad \vec{D}_f = \sum_i (c_i^f - c_i^{cd})/c_i^*$$



Small force
→Low improve capacity
→ High yield

Large force
→High improve capacity
→ Low yield

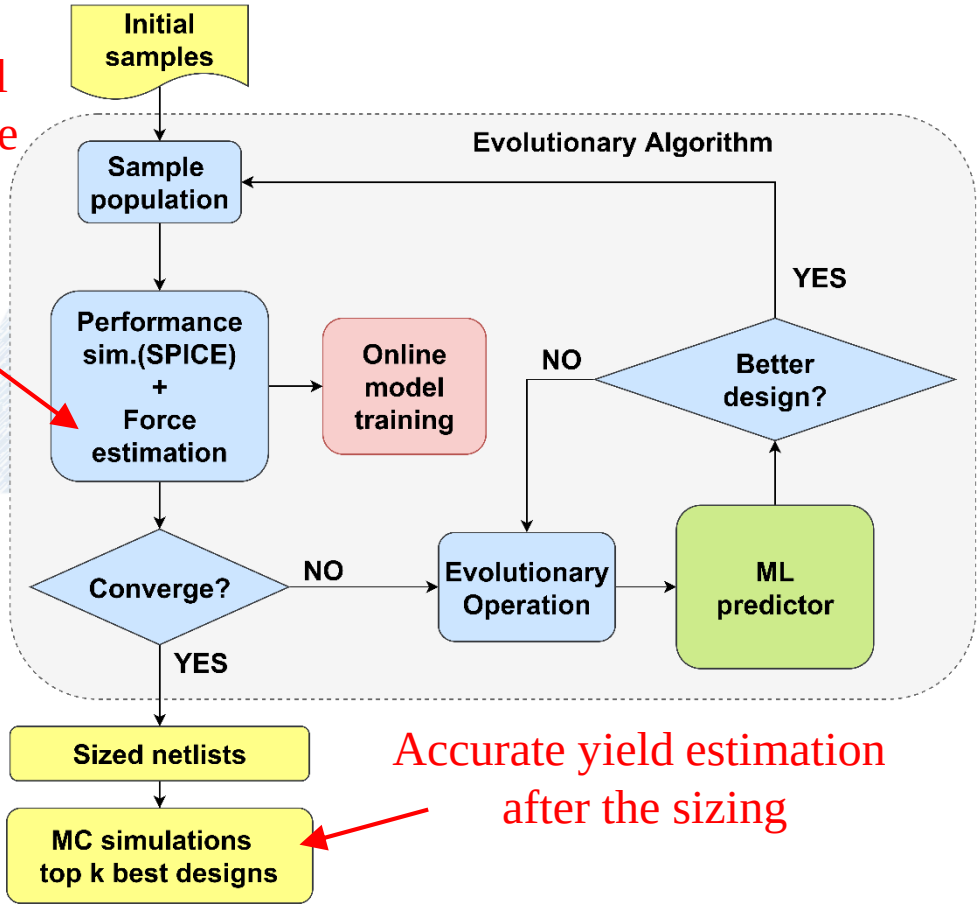
- Cannot give an accurate yield value
  - Will not scarify the solution too much
    - EA has good tolerance
  - Significantly reduce computation cost
    - No extra simulations are required

Methods	Monte Carlo	Force-directed model
Cost	Expensive → Costly simulations	Cheap → Simple equations
Yield Accuracy	Accurate value	Enough to rank

Sizing with Force-directed model

- Replace the MC analysis with force-directed model

Force-directed model replaces the expensive yield estimation



Cost function used in sample discarding:

$$cost(x) = \alpha * \sum_i w_i p_i(x) + \beta * F_{cd}$$

weighted performance

force score

Accurate yield estimation after the sizing

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Environment

- Implementation
  - Intel Xeon Gold 6248 CPU at 2.50GHz and 186GB memory
  - Python language and TensorFlow package
  - Simulator: Synopsys's HSPICE

- Sizing circuits
  - Two-stage operational amplifier (TSMC 0.18μm process)
  - Variable Gain Amplifier (TSMC 65nm process)
  - Analog-to-digital converter input buffer (TSMC 28nm process)

ML Model Analysis with OPA

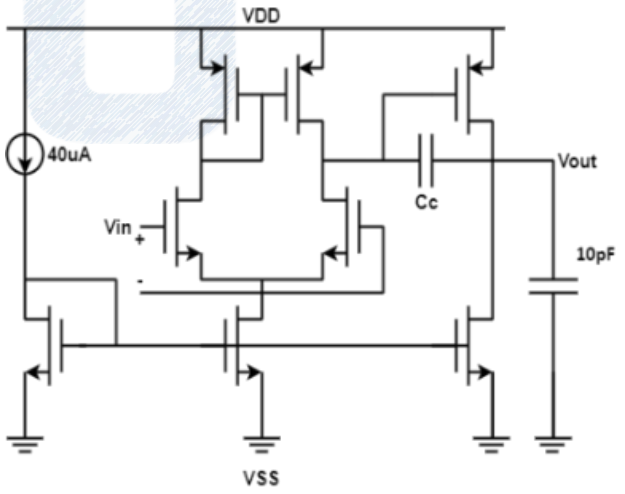
- Ensure the model can perform well in sizing flow

	Actual Positive	Actual Negative
Predict Positive	True Positive (TP)	False Positive (FP)
Predict Negative	False Negative (FN)	True Negative (TN)

$$\text{Accuracy} = \frac{(TP+TN)}{TP+TN+FP+FN} \qquad \text{Recall} = \frac{TP}{TP+FN}$$

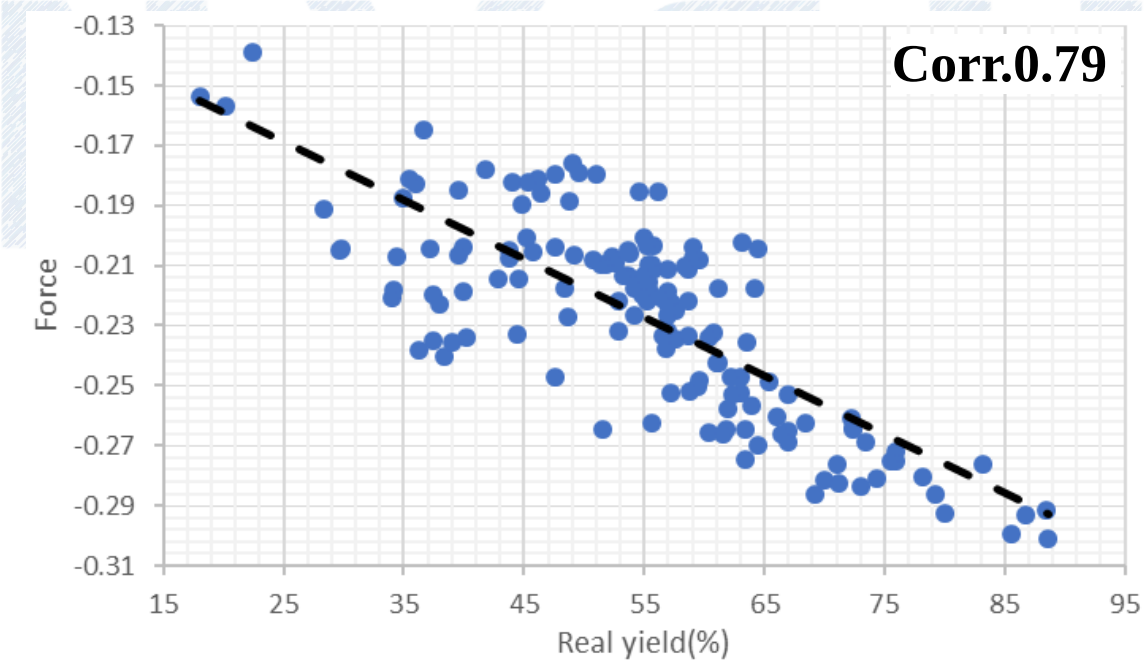
$$\text{F1 Score} = 2 * \frac{\text{Precision} * \text{Recall}}{\text{Precision}+\text{Recall}} \qquad \text{Precision} = \frac{TP}{TP+FP}$$

Two-stage OPA (TSMC 0.18um)			
Accuracy	Recall	Precision	F1 score
96.91%	81.29%	77.77%	0.7949



Force Model Analysis with OPA

- Verify the feasibility of the force-directed model
  - Clear trend between the force value and the real yield
    - Enough to guide the EA optimization
  - Much less simulation effort

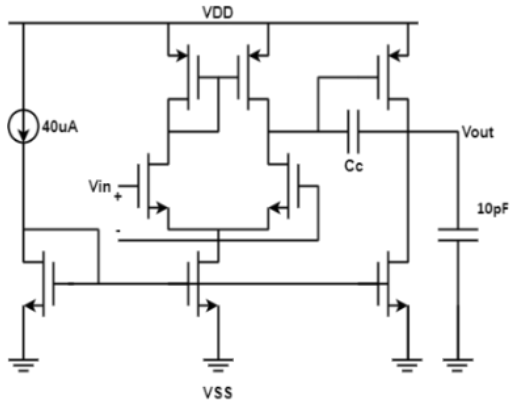


Two-stage OPA (TSMC 0.18um)

w/o DNN assisted
→Converge slower

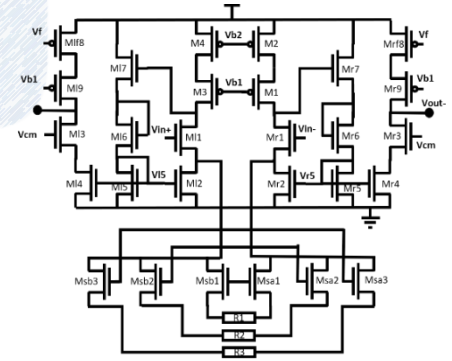
w/ DNN assisted
→Converge faster

Metrics	Spec	EA (w/o yield opt.)	EA +DNN	EA+DNN+ Force model(ours)
Gain (dB)	≥ 70	70.69	71.35	73.6
PM (°)	≥ 60	60.26	60.33	61.02
P_{DC} (μW)	≤ 1000	799.9	832.2	929.4
GBW (MHz)	≥ 5	5.36	5.37	5.56
SR (V/μs)	≥ 10	10M	10M	10M
#Iteration	--	292	30	**47**
#Total Sim.	--	10393	2009	**9554**
Yield(%)	--	34.5%	51.7%	**97.5%**



Variable Gain Amplifier (TSMC 65nm)

	EA (w/o yield opt.)	EA+MC	ORDE	EA +DNN+MC	EA+DNN+ Force model(ours)
Gain (dB)	18.07	19.02	18.68	19.50	18.88
PM (°)	92.27	95.54	96.06	95.83	96.00
P_{DC} (µW)	479.5	471.2	469.6	463.6	420.7
GBW (MHz)	8.22	8.10	8.03	9.04	8.22
#Training	-	-	-	50	**50**
#Iteration	45	140	138	36	**38**
#Perf. Sim.	1540	4580	4516	1252	**1316**
#MC Sim.	1000	561000	62620	258000	**8000**
#Total Sim.	2540	565580	67136	259252	**9316**
Speedup	-	1x	8.4x	2.2x	**60.7x**
Yield(%)	31.3%	96.1%	96.7%	97.8%	**97.4%**

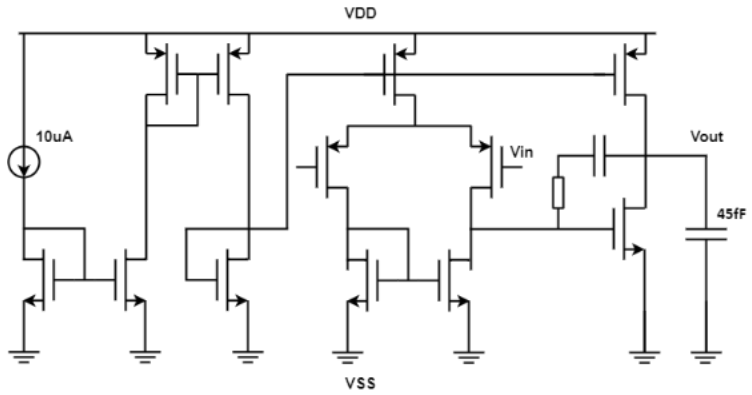


Force model replaces expensive MC
→ Higher speedup

ORDE: Bo Liu, Francisco V. Fernández, and Georges G. E. Gielen, "Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques", IEEE Trans. on CAD, vol. 30, Issue: 6, June 2011

ADC input buffer (TSMC 28nm)

	EA (w/o yield opt.)	EA+MC	ORDE	EA +DNN+MC	EA+DNN+ Force model(ours)
Gain (dB)	70.82	70.95	70.95	70.96	70.95
PM (˚)	85.22	85.13	85.16	85.33	85.26
#Training	--	--	--	50	50
#Iteration	94	189	179	36	41
#Perf. Sim.	3053	6098	5773	1202	1362
#MC Sim.	1000	733000	136155	388000	8000
#Total Sim.	4053	739098	141928	389202	9362
Speedup	-	1x	5.2x	1.9x	78.9x
Yield(%)	24.5%	92.1%	91.3%	94.5%	93.1%



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Conclusion

- Process variation is considered in the proposed ML-assisted EA optimization flow for analog circuit

- Significant speedup compared to the traditional variation-aware EA optimization
  - Reduce the number of simulations
    - ML screens out some useless designs and increase the converge ability
  - Reduce computational effort of each iteration
    - Force-directed model replaces the expensive MC simulation

Thank You!