A 2.17μW@120fps Ultra-Low-Power Dual-Mode CMOS Image Sensor with Senputing Architecture

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Outline

- **Motivation & Background of Research**
- **Overall Architecture of Proposed Senputing CIS Sensor**
- **Detailed Circuit Design**
- **Implementation Results & Demo System**
- **Summary**

Motivation

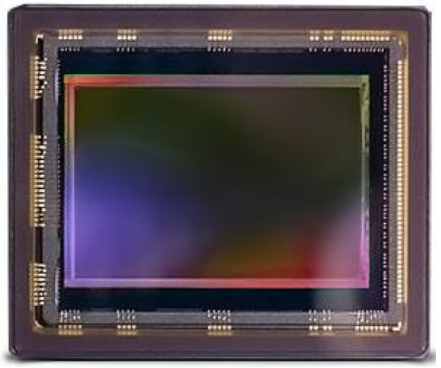
■ **Needs for Intelligent Vision Device Increases**

Robot

Field Observation

AI Glasses

- **Deployed on the edge**
- **Working for 24 hours (Always-on)**
- **Battery-powered**
- **Huge power consumption**



CMOS Image Sensor

Recently, Hierarchical always-on visual system is proposed to solve power problem

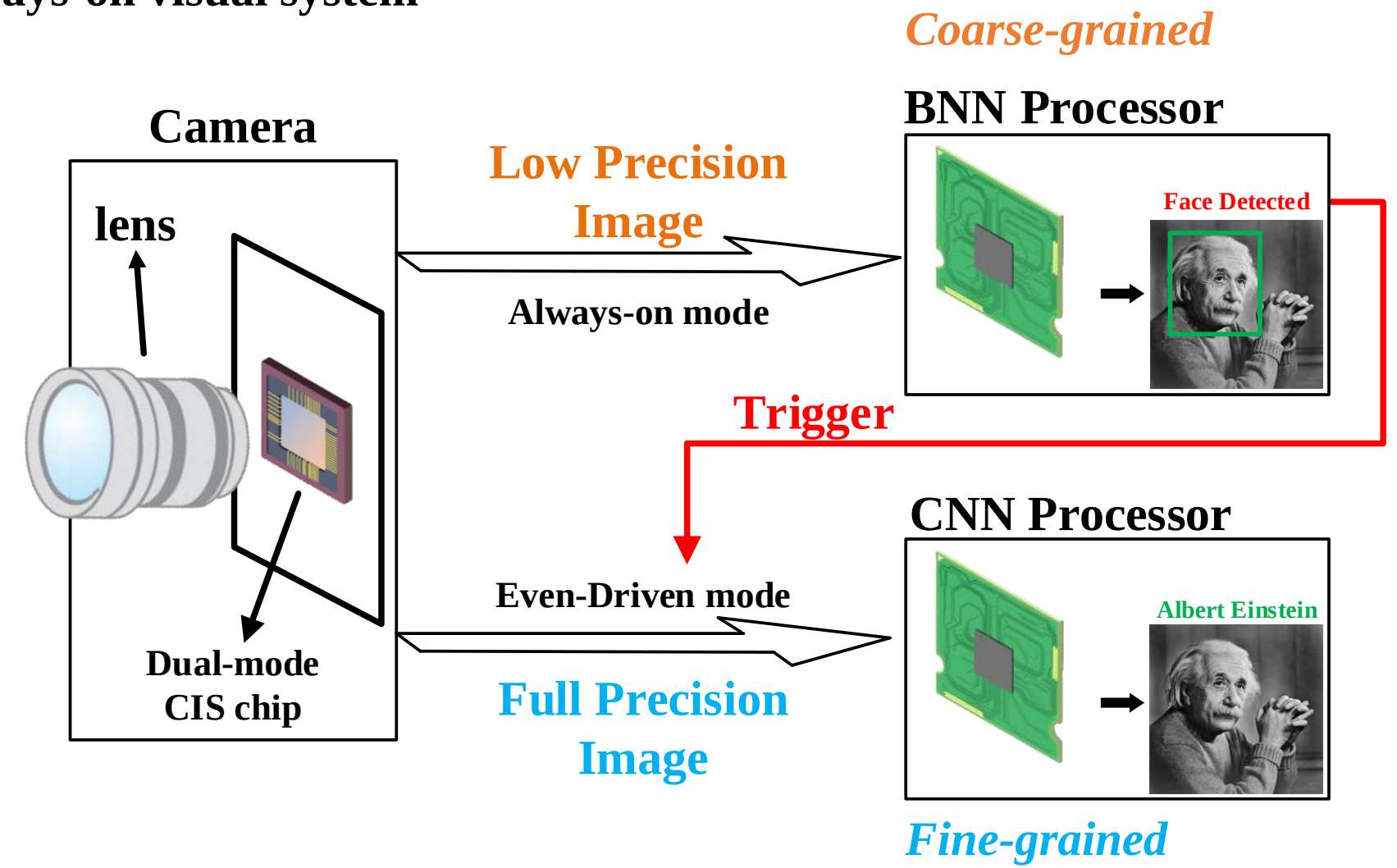
Background Overview

■ **Typical hierarchical always-on visual system**

➢ **Two working modes:**

- **Always-on**
- **Event-driven**

➢ ***What we concerned ?***



Background Overview

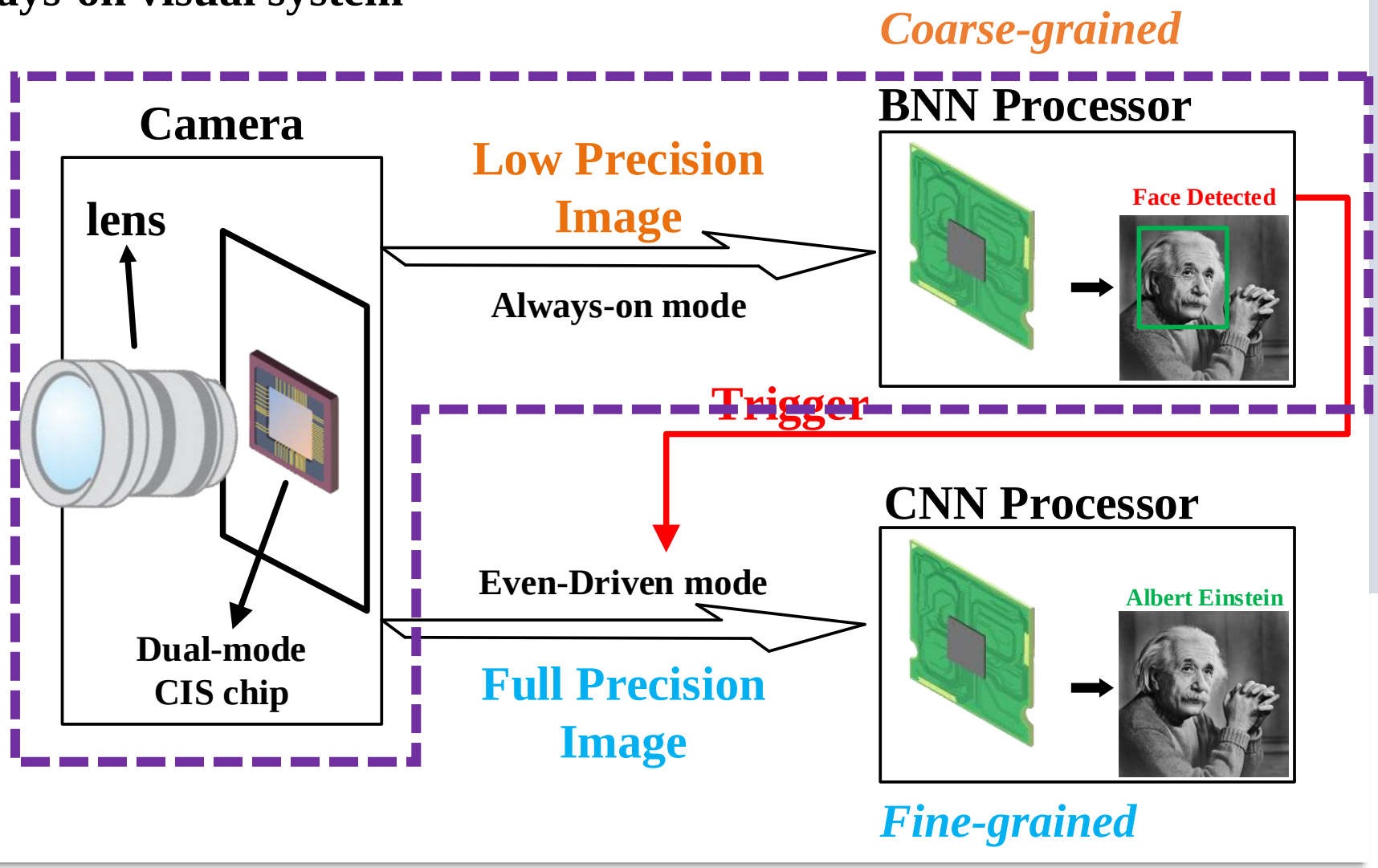
■ **Typical hierarchical always-on visual system**

➢ **Two working modes:**

- **Always-on**
- **Event-driven**

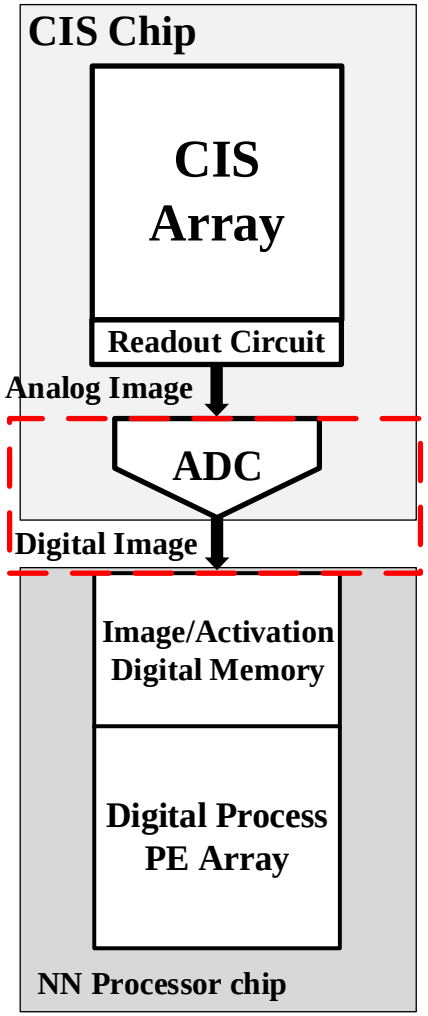
➢ ***What we concerned ?***

Power of always-on mode



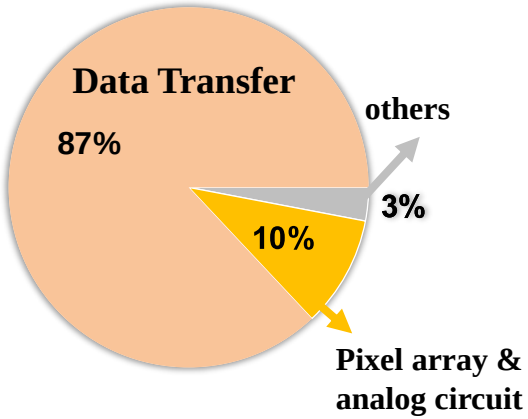
Background Overview

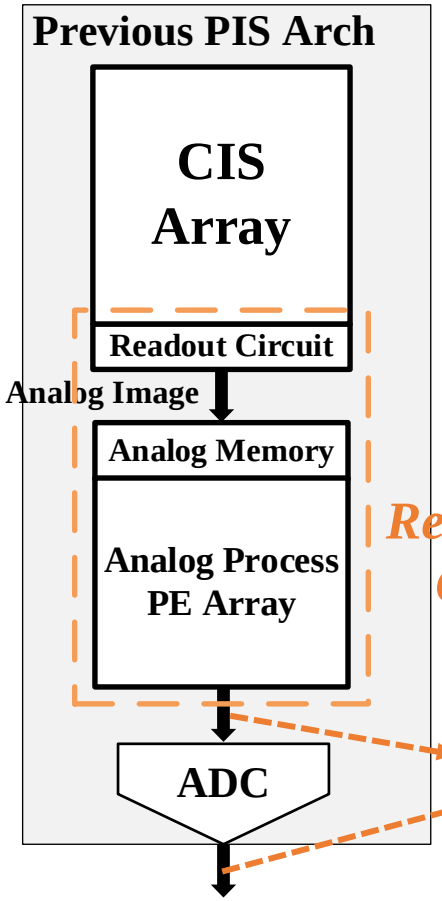
■ Traditional image processing flow vs Previous PIS Architecture



- Separated
- A→D Convert
- Digital Image Out

High-throughput!





- Integrated
- Still A→D Convert
- Digital Feature Map Out

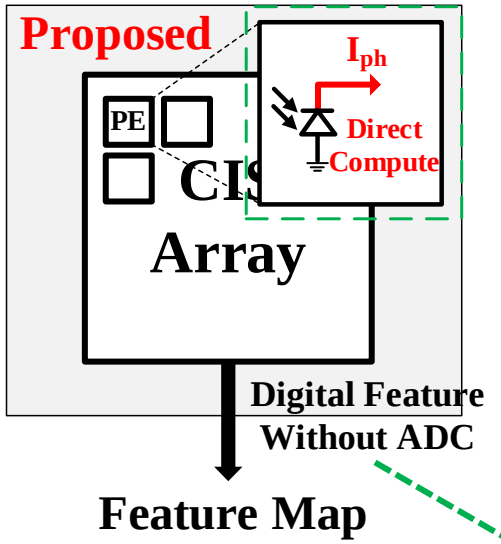
Redundant Power Consumption

Low-throughput

Reference :

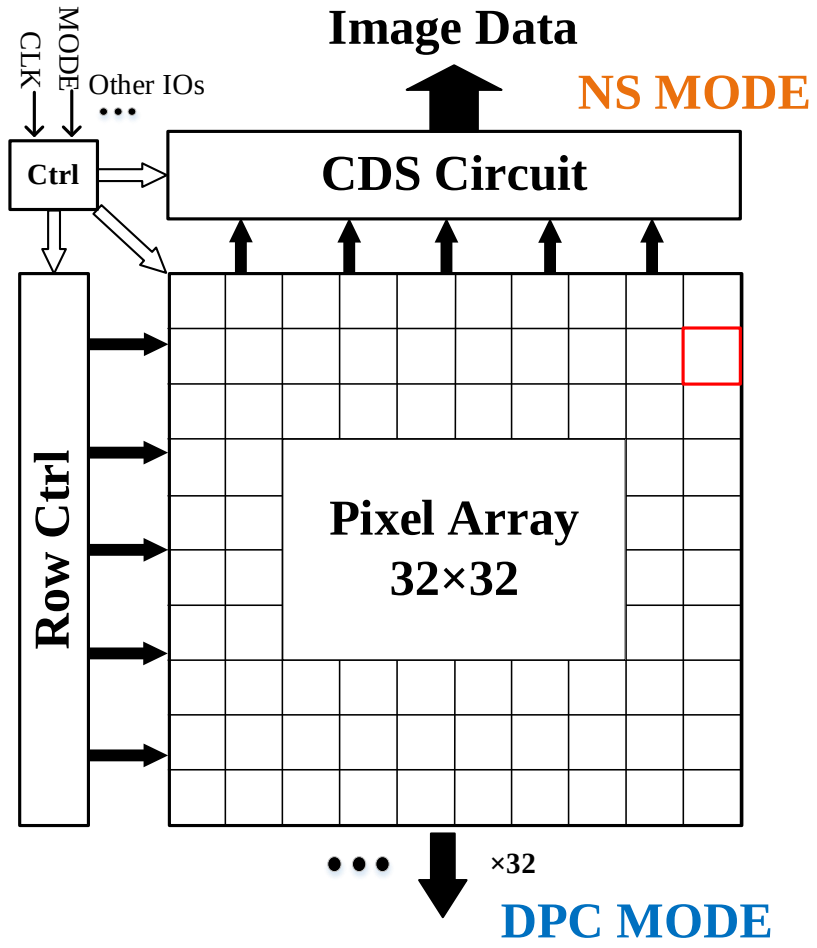
Proposed Architecture

■ Proposed Sensing-with-computing (Senputing) Architecture



- Implement *MAC* inside per pixel
- Eliminate A→D Convert
- Output binary feature map

Ultra-Low throughput



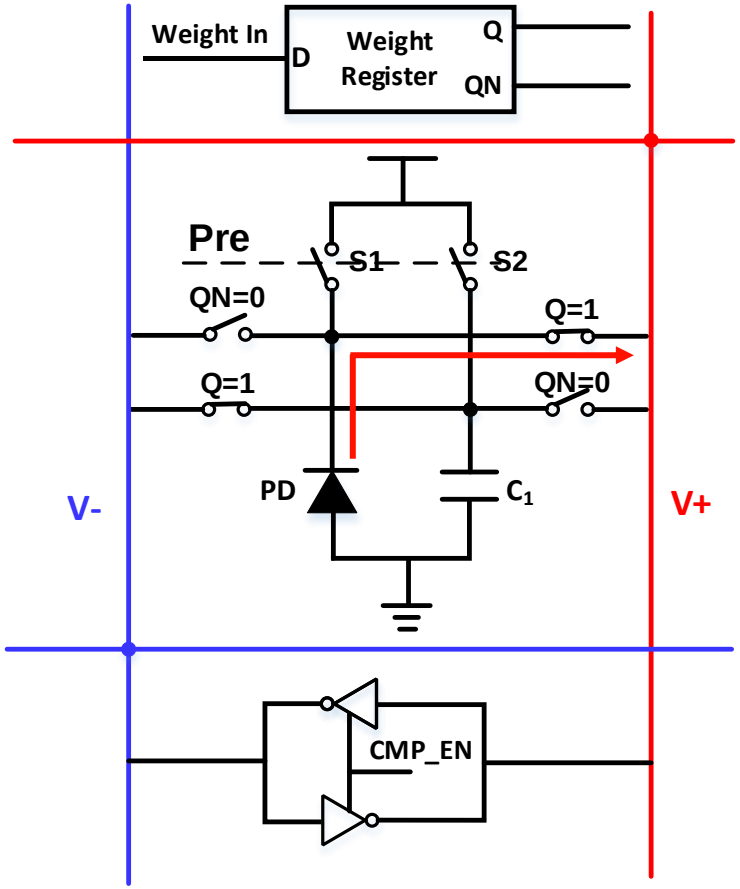
- Two working modes: (Both 32x32)

1. Normal Sensor Mode

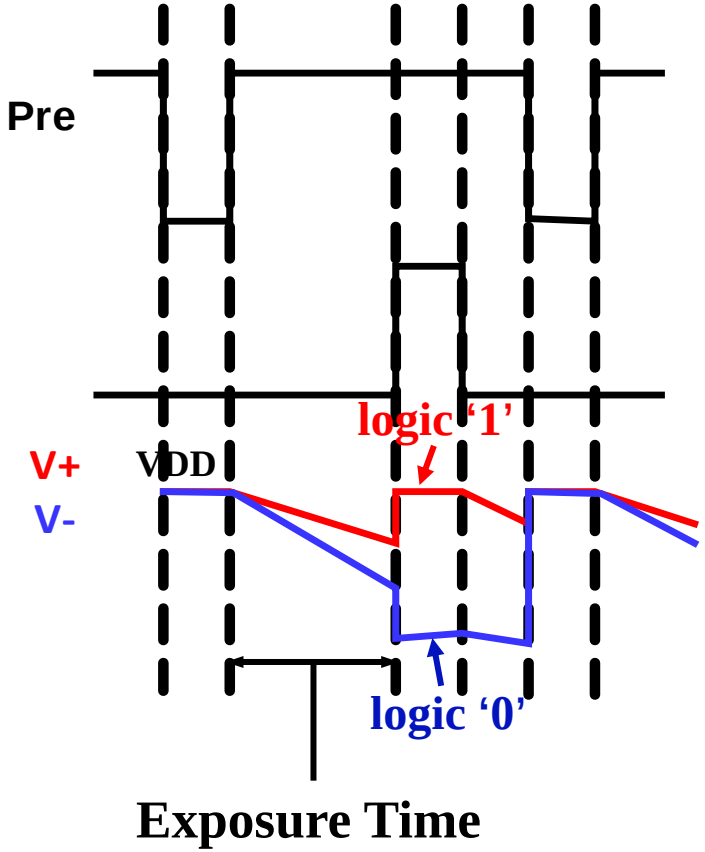
2. Direct Photocurrent Computation Mode

Concept of Senputing

■ MAC Operation Circuit inside Pixel (DPCE)



- Q = 1 , PD→V+;
- Q = 0 , PD→V-;
- $C_{PD} = C_1$

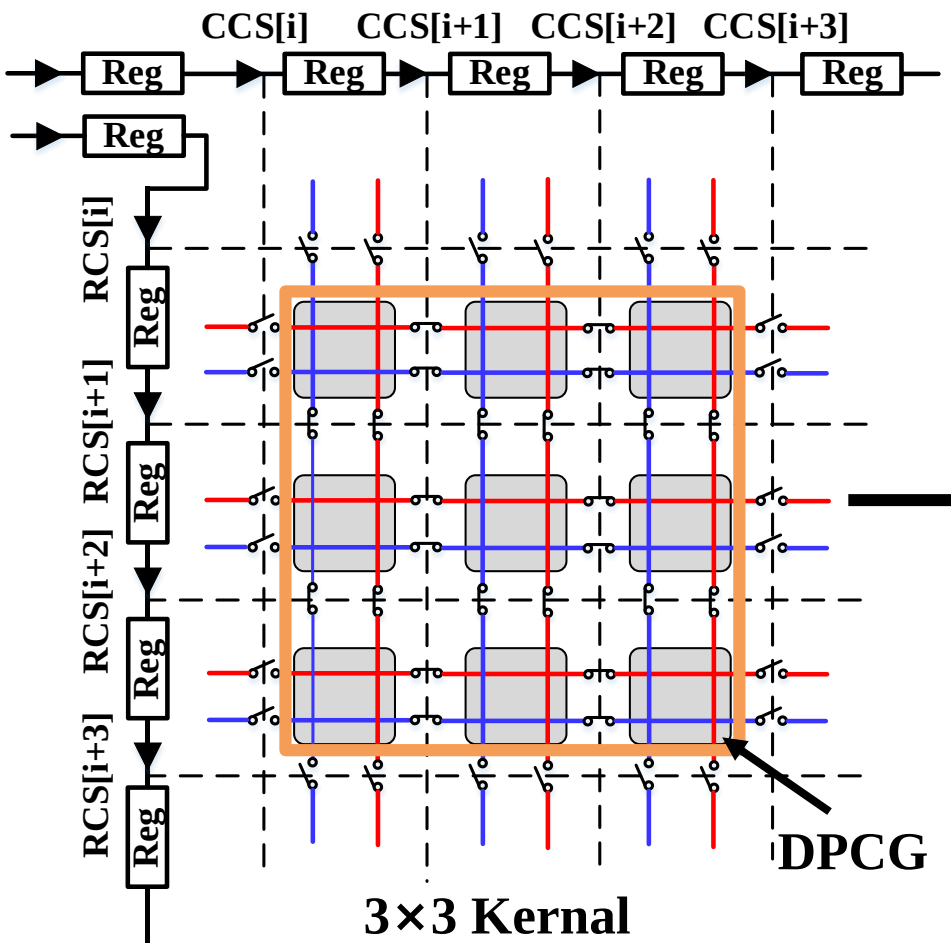


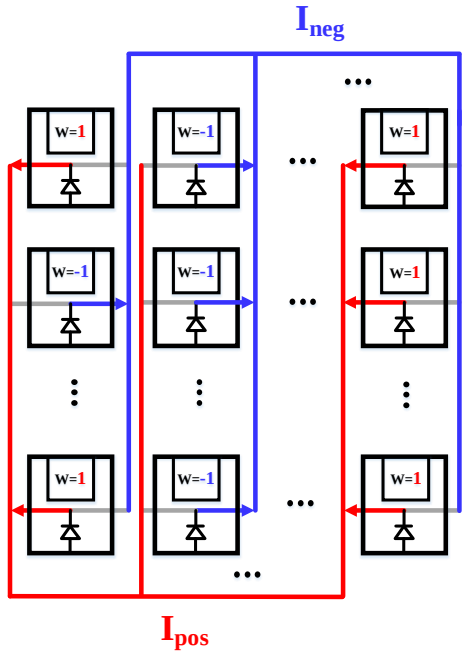
ΔV+ < ΔV-, set V+ to logic '1'

ΔV+ > ΔV-, set V+ to logic '0'

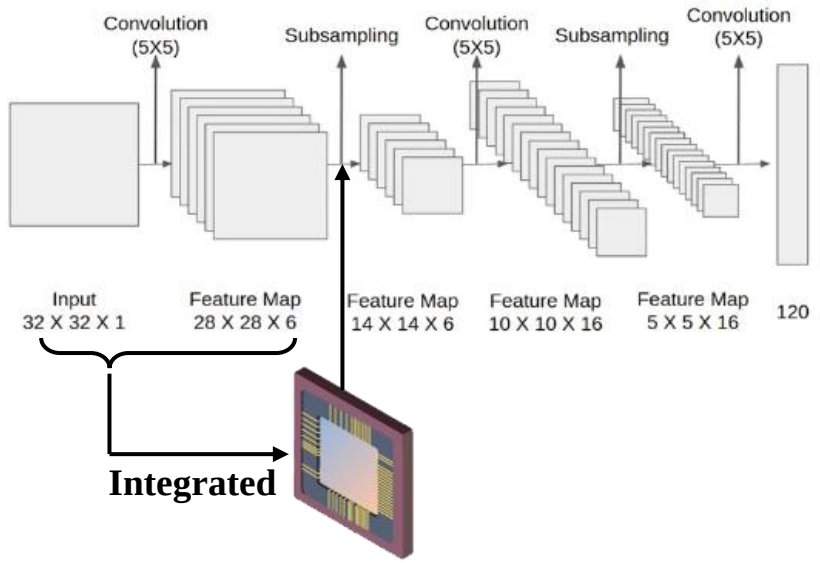
MAC Operation

■ Configurable Kernel Size





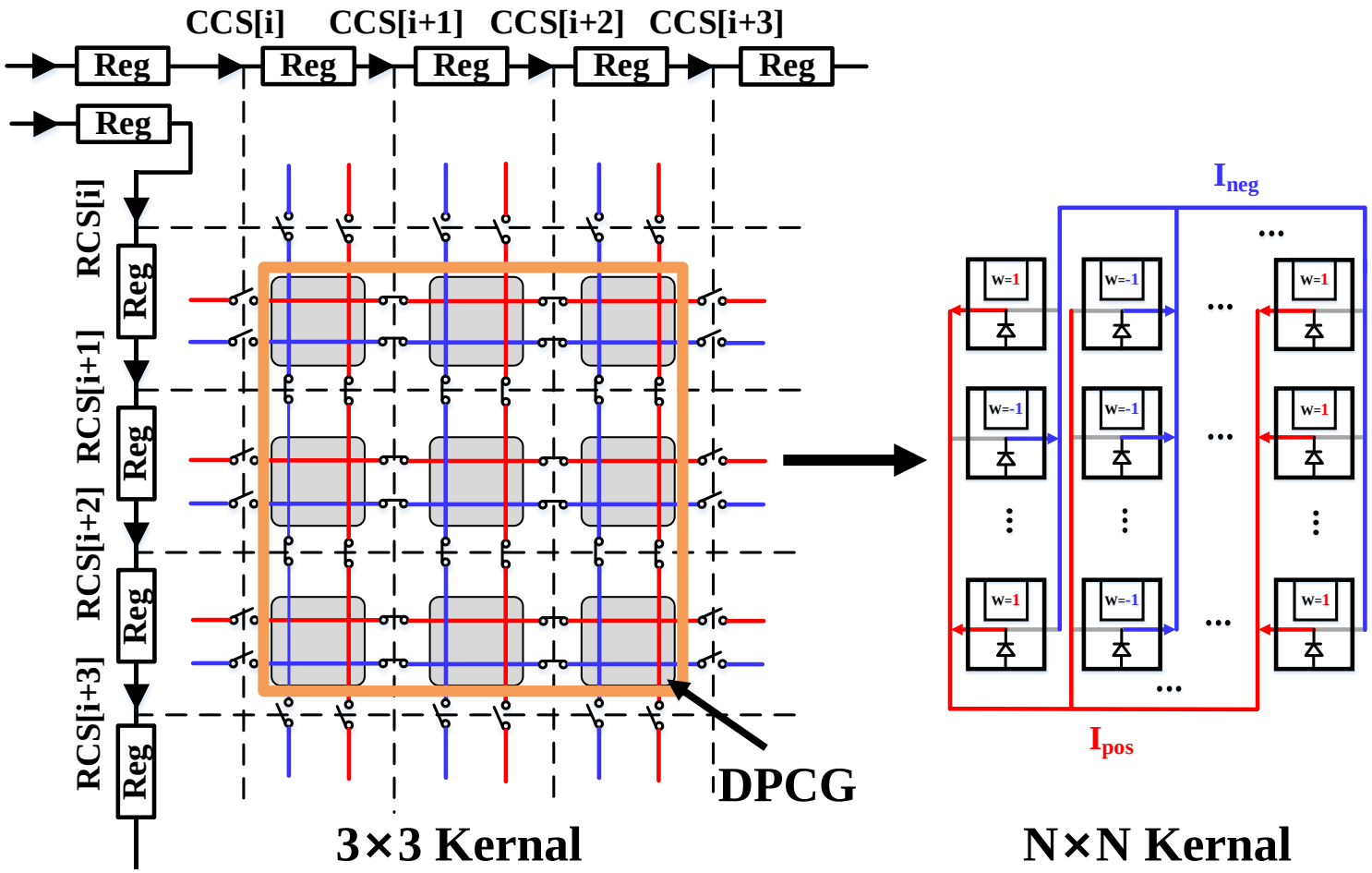
Lenet-5



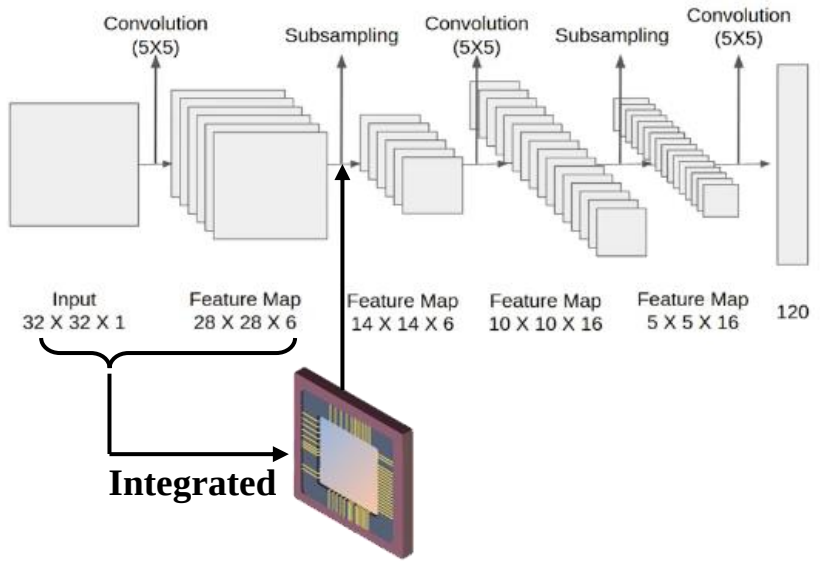
$$y = sign[1 \times \sum_{x_i \in X_1} x_i + (-1) \times \sum_{x_i \in X_2} x_i]$$

MAC Operation

■ Configurable Kernel Size



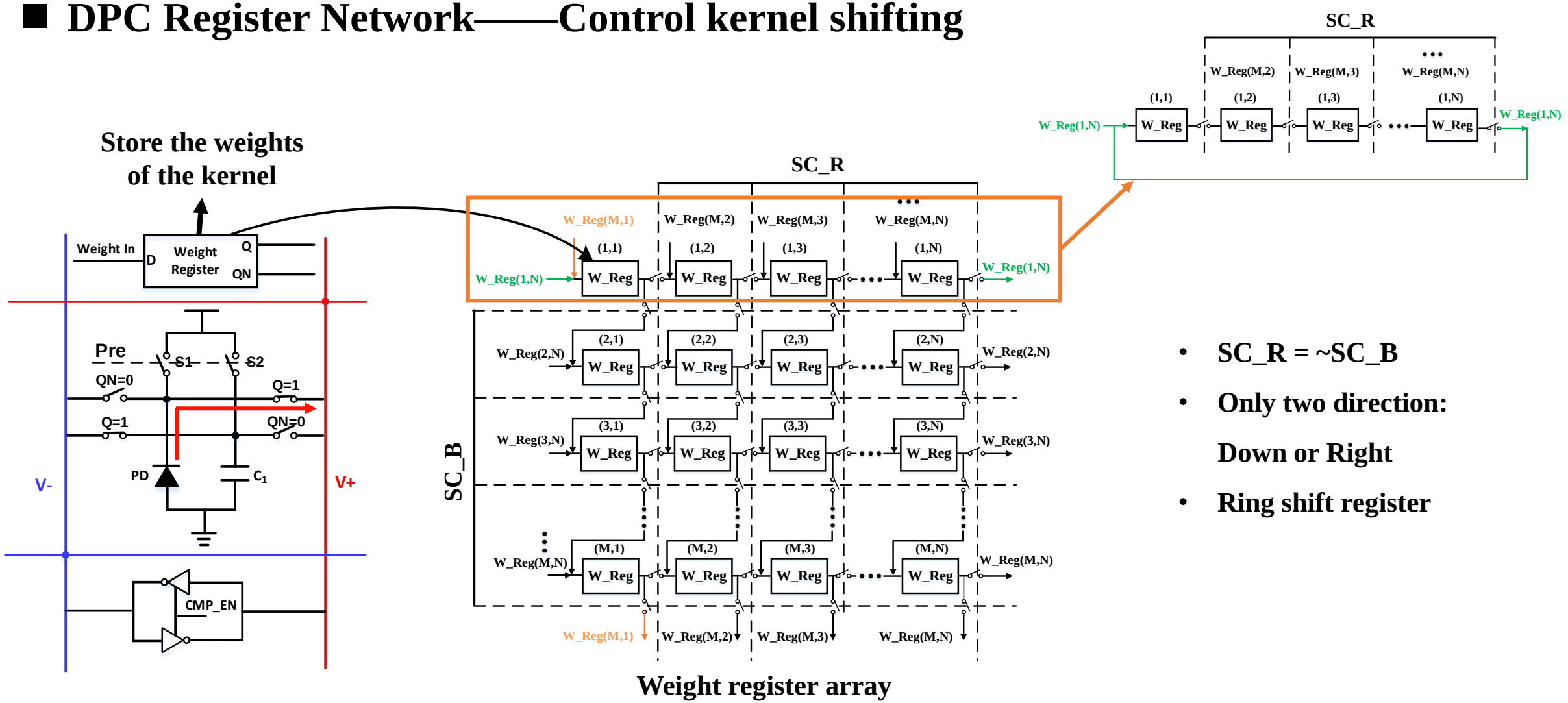
Lenet-5



How to obtain the whole 6 × 28 × 28 feature map?

MAC Operation

■ DPC Register Network——Control kernel shifting

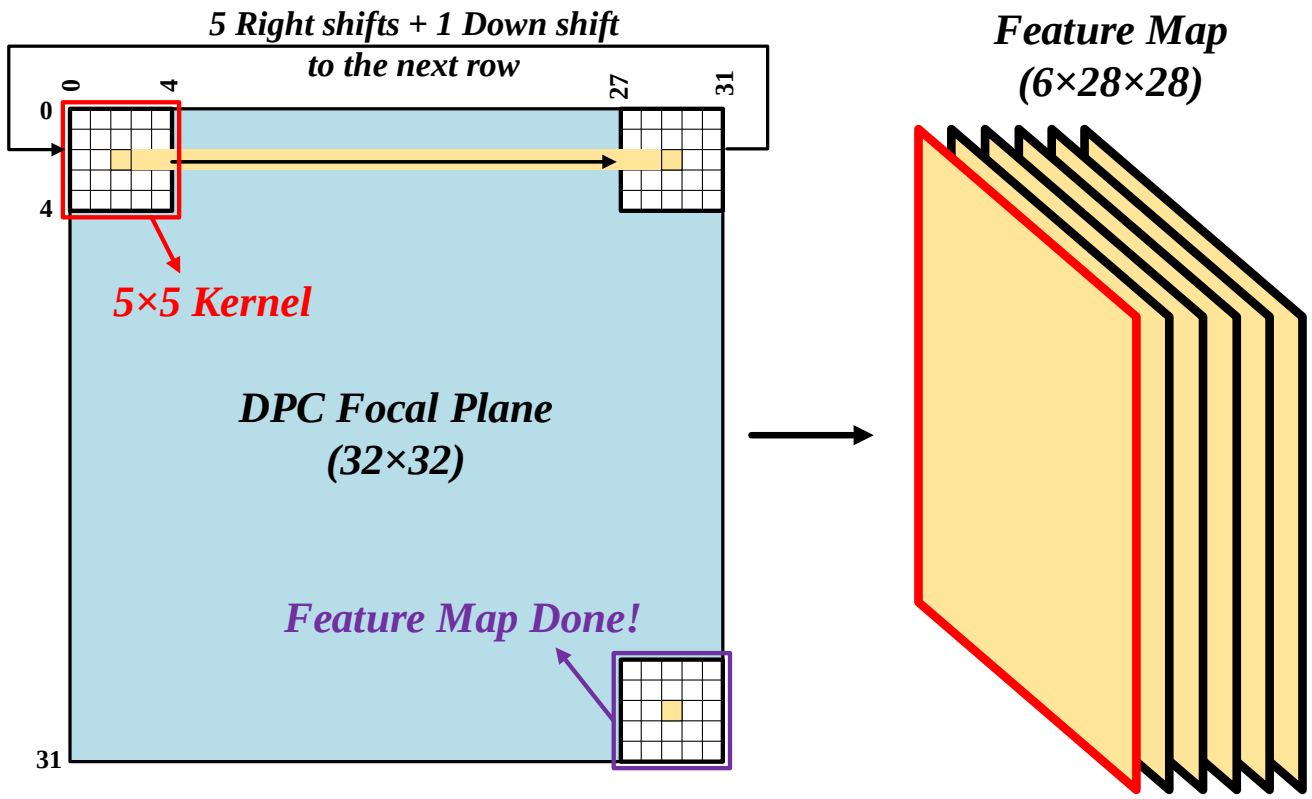


- SC_R = ~SC_B
- Only two direction:

  Down or Right
- Ring shift register

MAC Operation

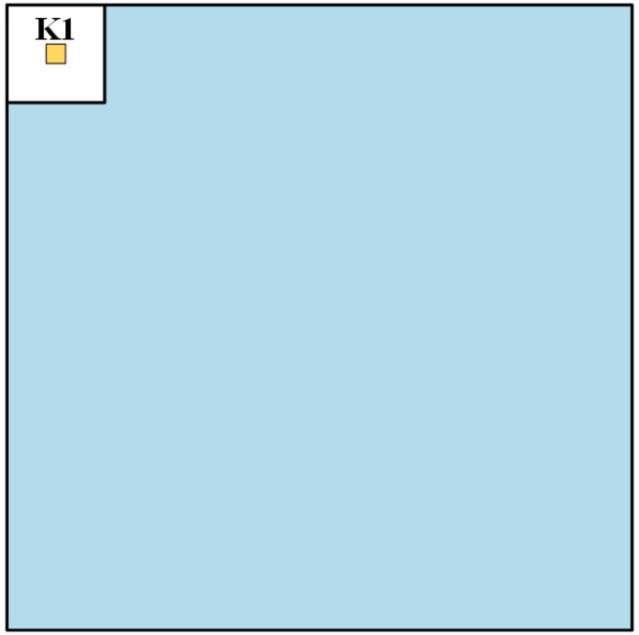
■ Kernel Shifting Flow



1 row : 28 right_shift

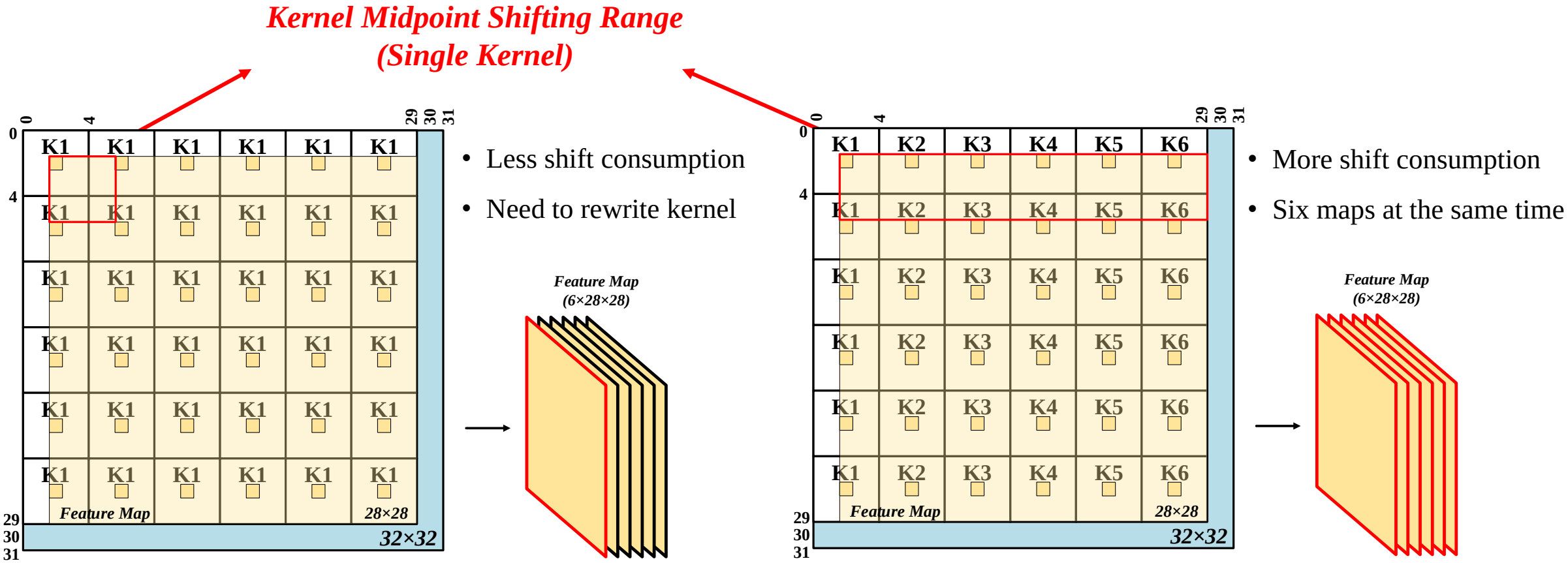
Reset : 5 right_shift + 1 down_shift

Total : 32×28 + 27 shifts



MAC Operation

■ Simplified Shifting Schedule

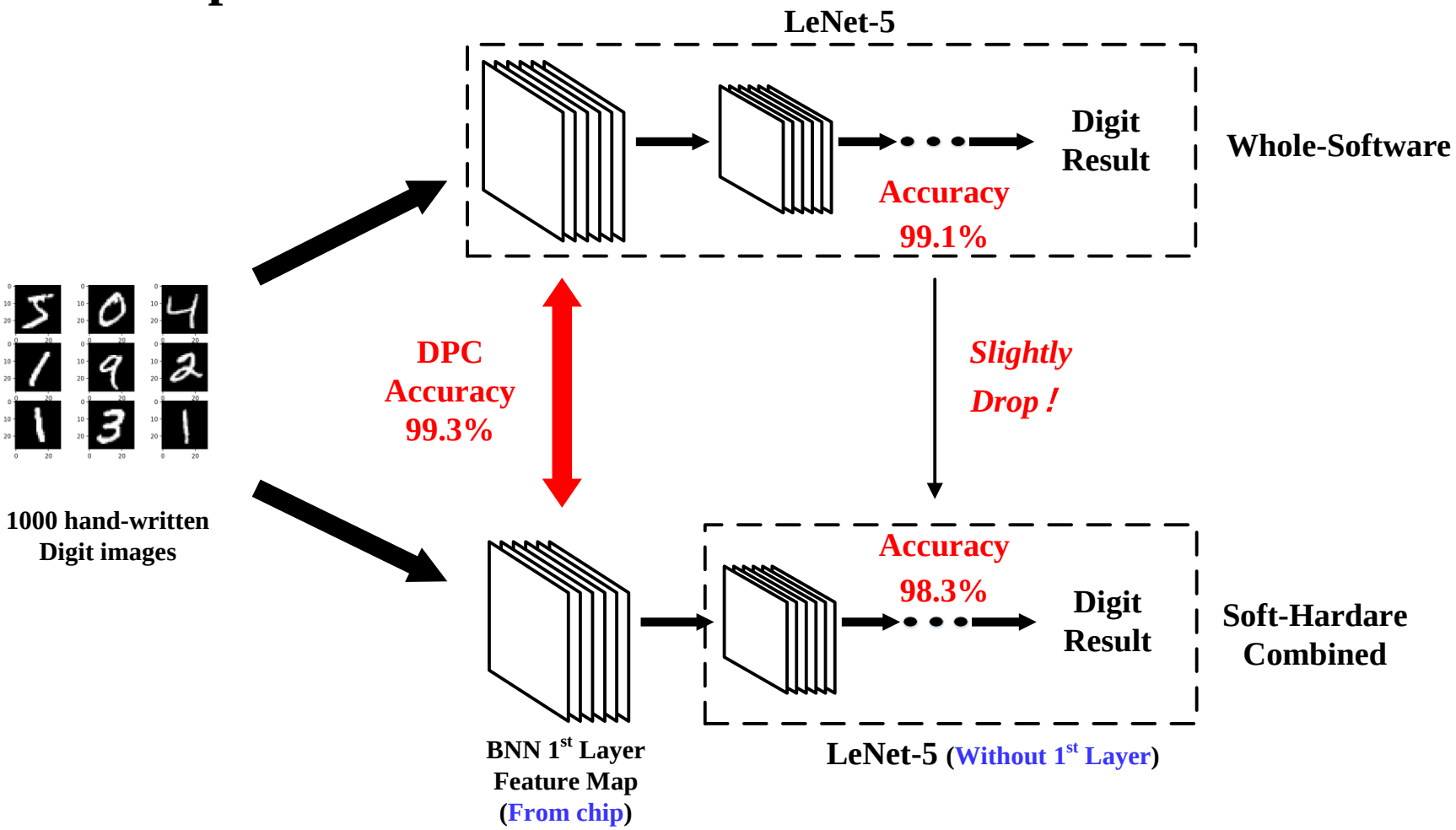


- Less shift consumption
- Need to rewrite kernel

- More shift consumption
- Six maps at the same time

Implementation Results

Performance Comparison



DPC Accuracy: The accuracy of DPC circuit calculation for BNN 1st-layer feature map

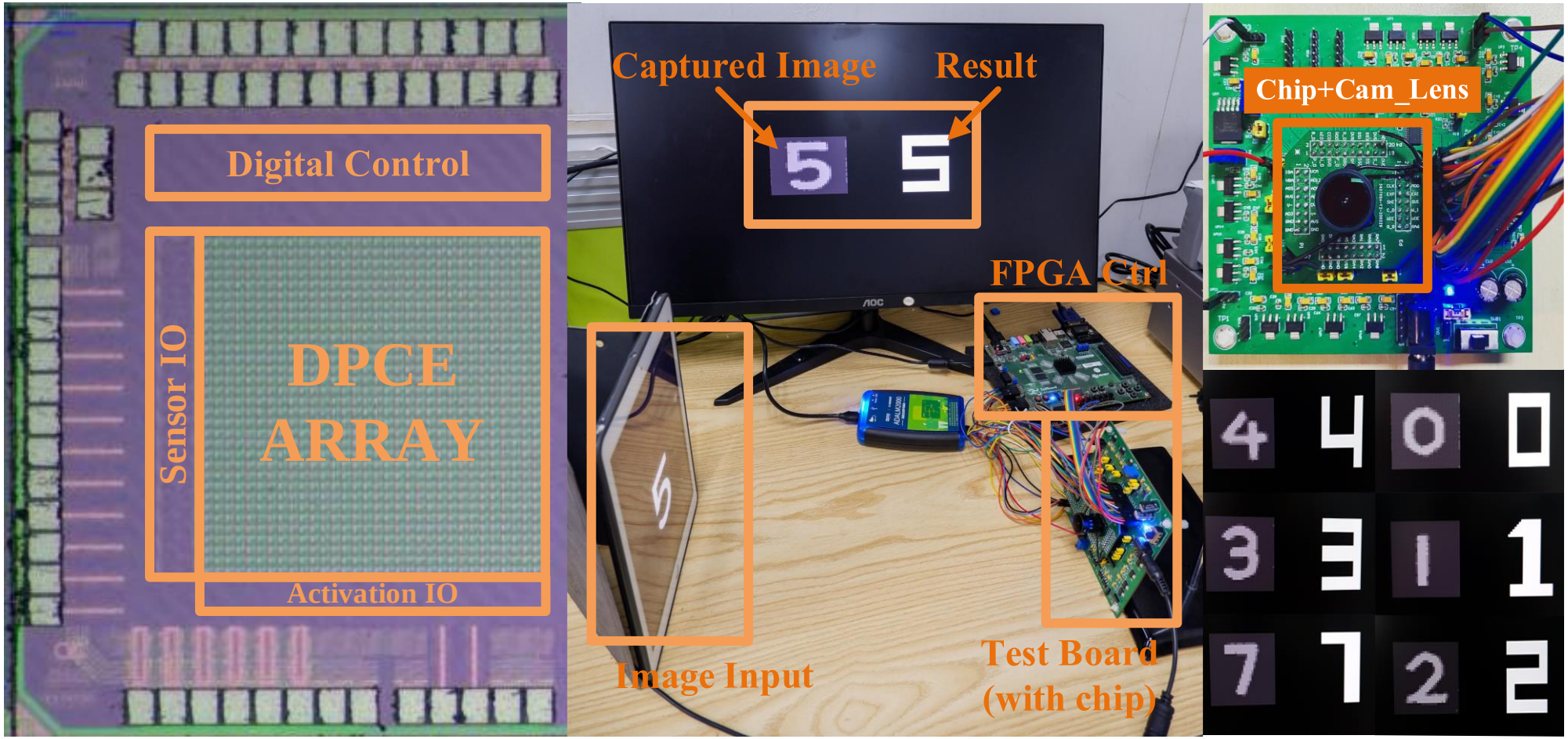
Implementation Results

■ Performance Comparison

	TIE2020[4]	ASSCC2019[1]	ISSCC2021[2]	TCASI2019[3]	This Work
Process	180nm	180nm	65nm	180nm	65nm
Pixel Pitch	6.5um	7.6um	9um	40um	20um
Array Size	192×128	128×128	160×128	32×32	32×32
Framerate	312.5 fps	480 fps	24~268 fps	100 fps	120 fps
Feature	BNN 1st-layer	CNN 1st-layer	CNN 1st-layer	Binary CNN	BNN 1st-layer
Weight	Fixed	Programmable	Programmable	Programmable	Programmable
Accuracy	96.7%@MNIST	N/A	RMSE=4.1%	99%@MNIST	98.1%@MNIST
Kernel Size	2×2~8×8	3×3	$2^N \times 2^N (N<6)$	5×5	Mixed
Power	52.5 mw	Image: 77uW Conv: 91uW	42~256uW	1.8mW	2.14uW
Efficiency (Ops/W)	$555G^2$	1.51T	$0.15\sim3.64T^2$	545G	$11.49T^2$

Implementation Results

- **Chip micrographs & Demo System**



Summary

- **Proposed a dual-mode CIS chip with dual-resolution**
- **Implement Direct Photocurrent Computation inside pixels —— Senputing**
- **Design several kernel shifting methods**
- **Compare the performance of proposed CIS chip**
- **Demo system base on the Senputing CIS chip**

Thanks for your listening

Q & A Time