Supply-Variation-Tolerant Transimpedance Amplifier Using Non-Inverting Amplifier in 180-nm CMOS

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Outline

- Background
- Comparing the reference TIA and the proposed TIA
- Design of the proposed TIA
- Measurement result
- Conclusion

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Overview of Optical Communication Systems

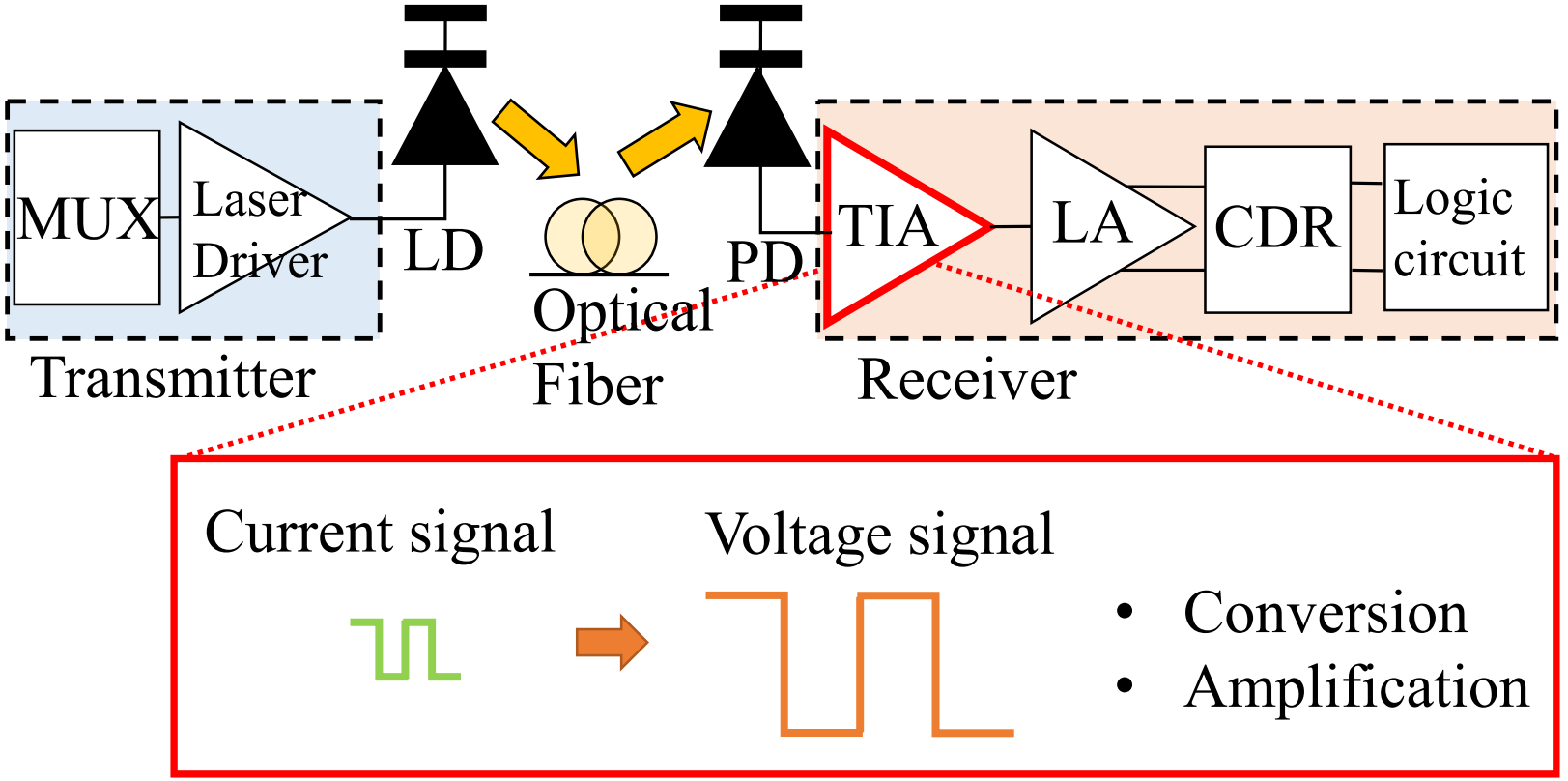


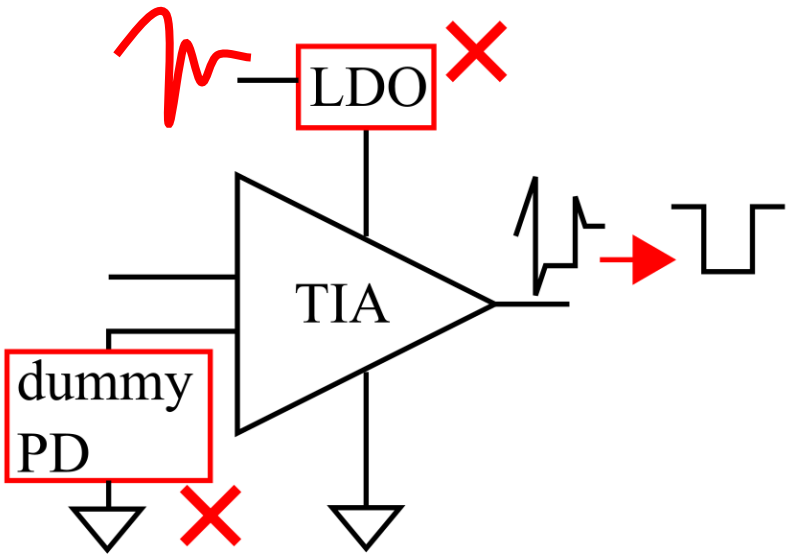
Fig. Overview of Optical Communication Systems.

Power Supply Noise Affects TIA Output.

➡ The bit error rate increases.

Power supply noise reduction

Commonly, power supply noise reduction uses extra circuits.



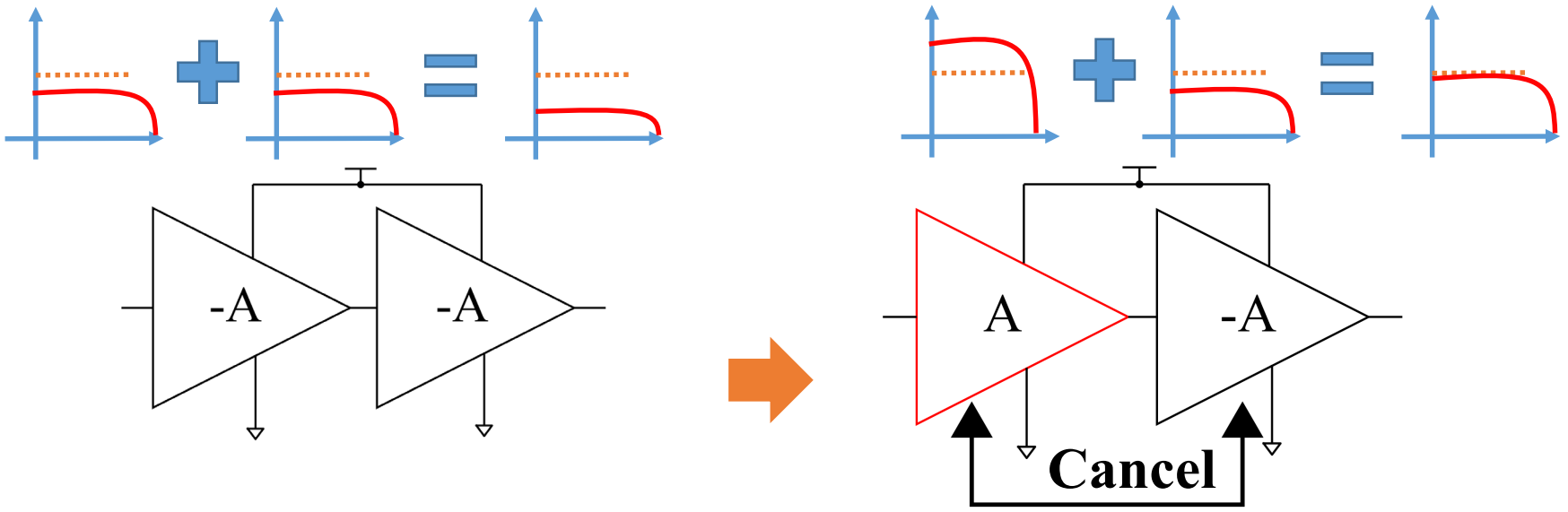
High performance extra circuits increase the costs.

- Power consumption
- Area
- Another power supply

We realize Supply-noise-tolerant TIA without extra circuits.

Our key idea

Invert the characteristic of circuit.



How we invert the characteristic of TIA?

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The reference TIA

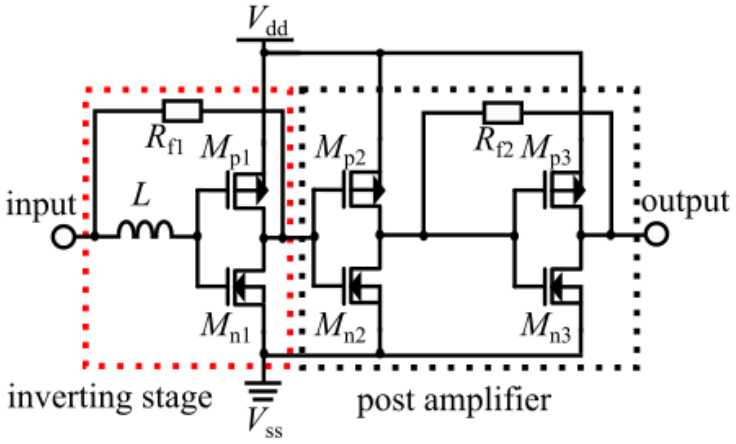

Fig. Schematic of the reference TIA.

A combination of a inverting stage and post amplifier

The gain of the inverting stage

$$g_m R_f$$

The supply voltage drops and the current through the MOS decreases.

The gain of the inverting stage and post amplifier decrease.

The combination of a circuit that increases gain when the current decreases.

The proposed TIA

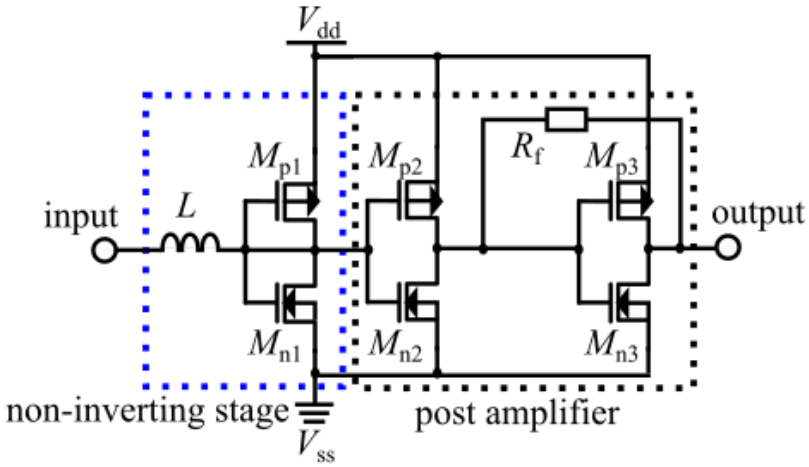

Fig. Schematic of the proposed TIA.

A combination of a non-inverting stage and post amplifier

The gain of the non-inverting stage

$$\frac{1}{g_m}$$

By supply voltage drop

- The gain of the non-inverting stage increases.
- The gain of post amplifier decreases.

Cancel out the effects of power supply voltage drop

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Evaluation in simulation

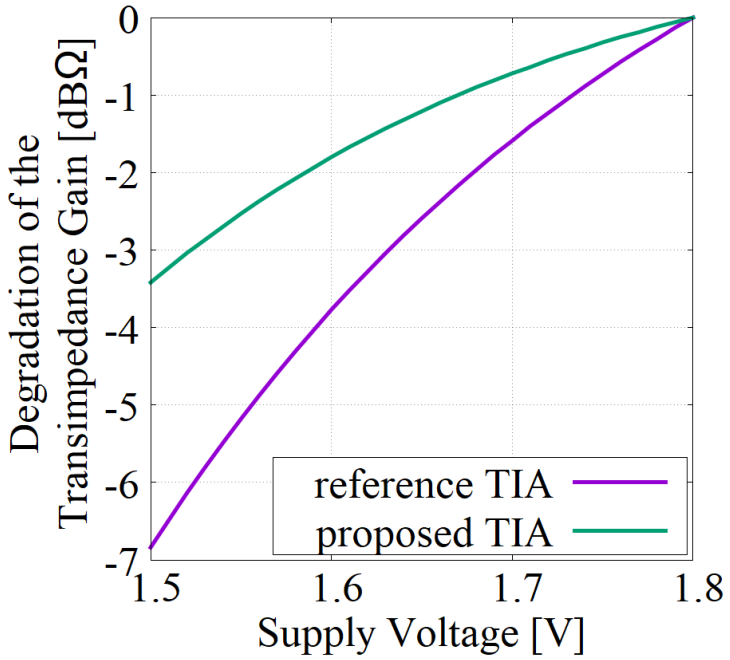


Fig. Characteristic of the supply voltage-Degradation of the gain.

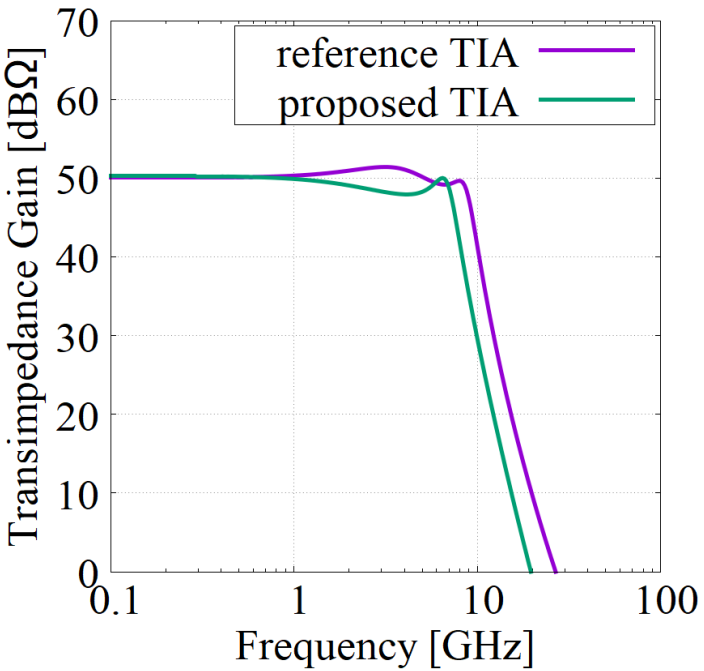


Fig. Frequency characteristics.

Merit：Tolerance to power supply variations

Demerit：Degradation of bandwidth

Eye diagram of proposed TIA at 1.5V is good.

Design of the proposed TIA

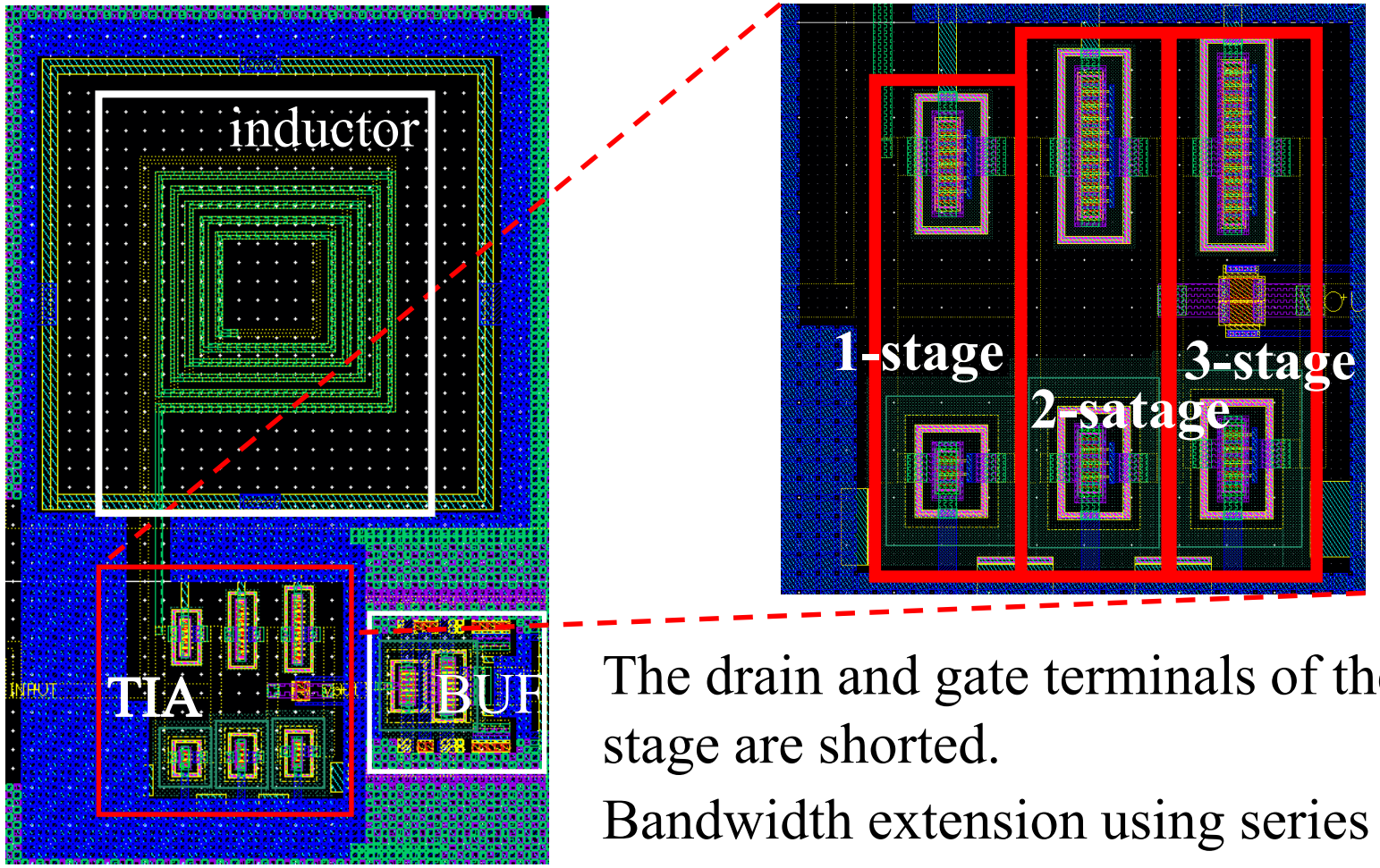


Fig. Layout view of the proposed TIA and the output buffer.

The drain and gate terminals of the first stage are shorted.

Bandwidth extension using series peaking

Design parameters

Design parameters (reference TIA)

M_{n1}	M_{p1}	M_{n2}	M_{p2}	M_{n3}	M_{p3}
10 μm	36 μm	10 μm	28 μm	12 μm	34 μm

resistance R_{f1}, R_{f2}	inductance L
350 Ω	4 nH

Performance (reference TIA)

Power consumption : 6 mW
Gain : 50 dBΩ
Bandwidth : 9.0 GHz

Design parameters (proposed TIA)

M_{n1}	M_{p1}	M_{n2}	M_{p2}	M_{n3}	M_{p3}
6 μm	20 μm	12 μm	36 μm	14 μm	42 μm

resistance R_f	inductance L
300 Ω	7 nH

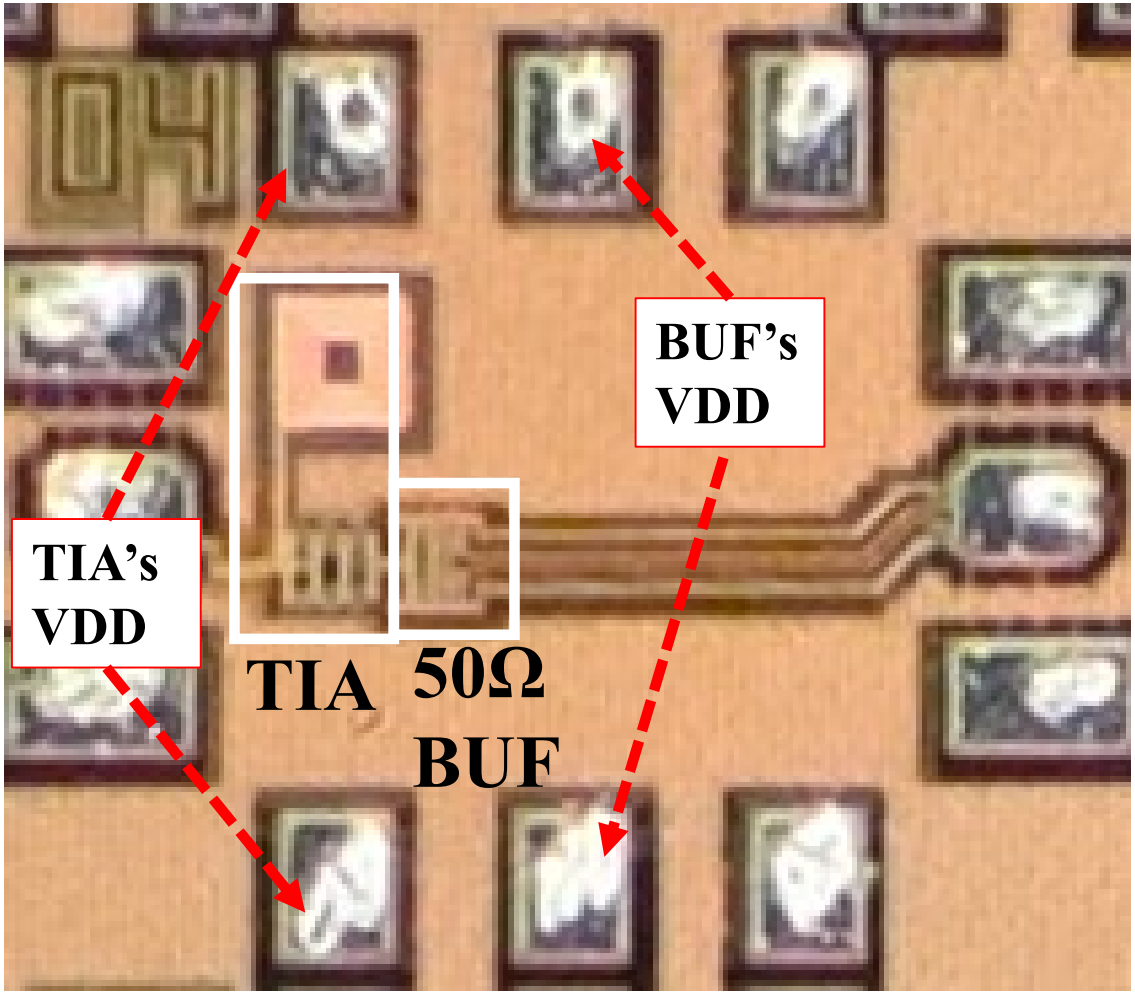
Performance (proposed TIA)

Power consumption : 6 mW
Gain : 50 dBΩ
Bandwidth : 7.3 GHz

Constraints : 50 dBΩ, 6 mW

Designed for high power supply variation tolerance.

Overview of the chip design



- 180-nm CMOS
- On-wafer probing

Fig. Chip microphotograph of TIA and output buffer.

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Measurement set up (1)

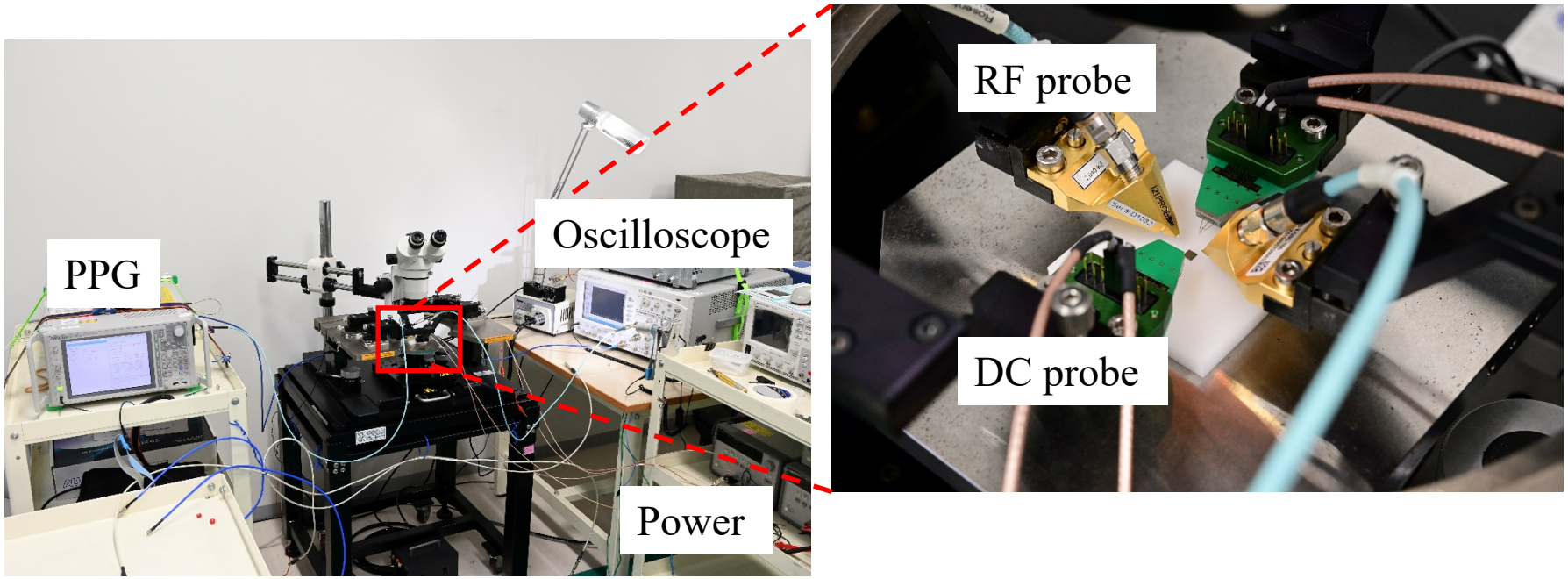
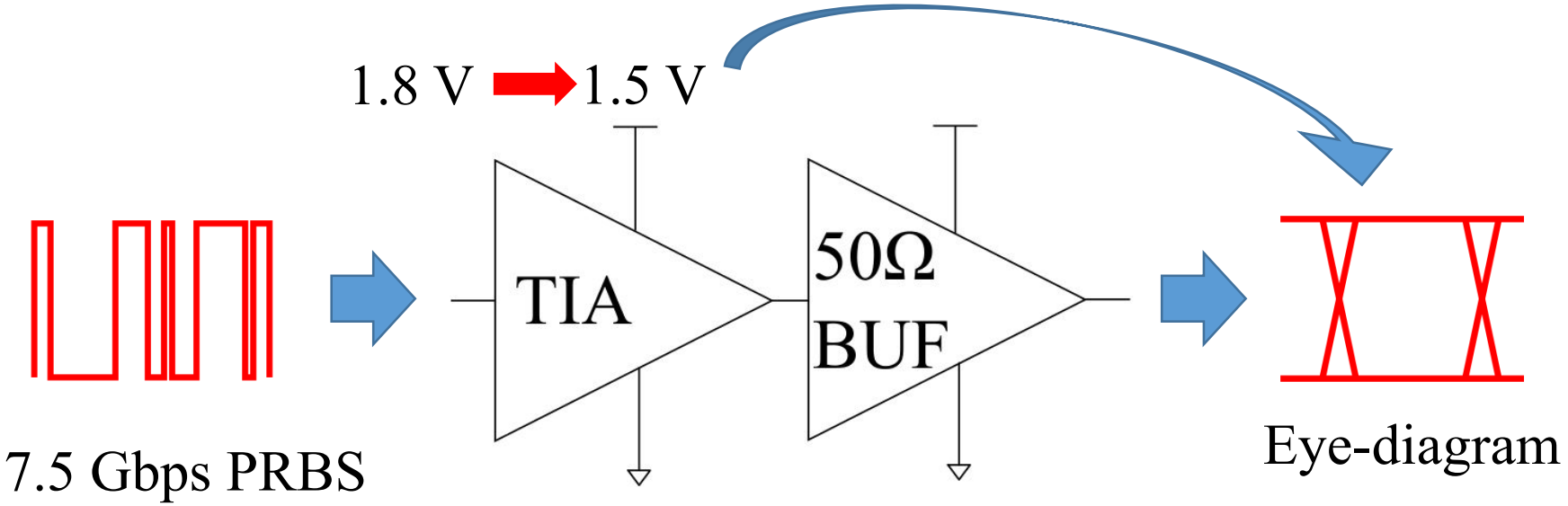


Fig. Photo of the measurement system.

- Generate PRBS with Pulse Pattern Generator (PPG)
- Measure eye diagram with oscilloscope

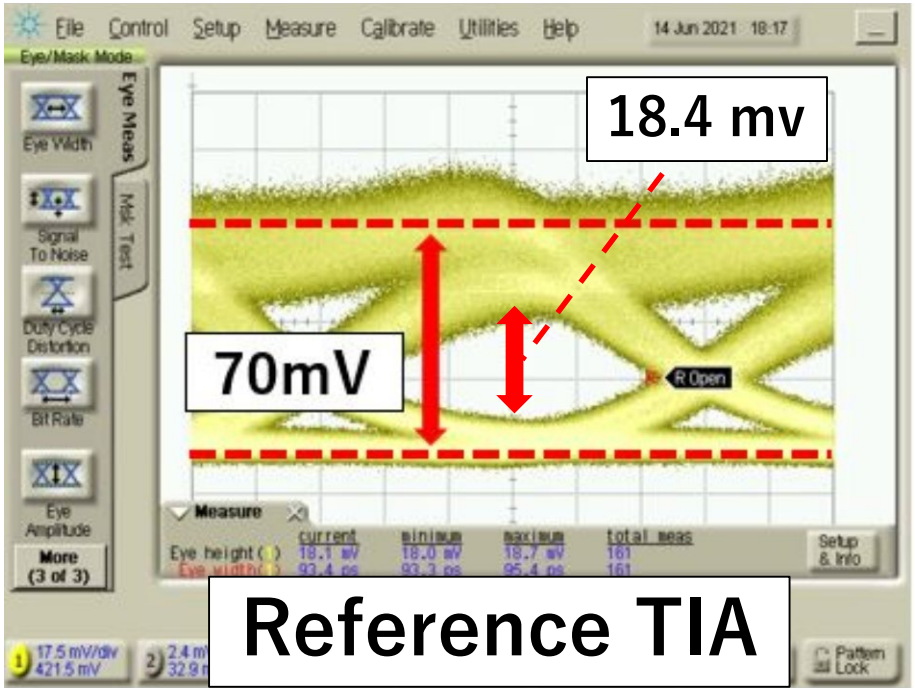
Measurement set up (2)

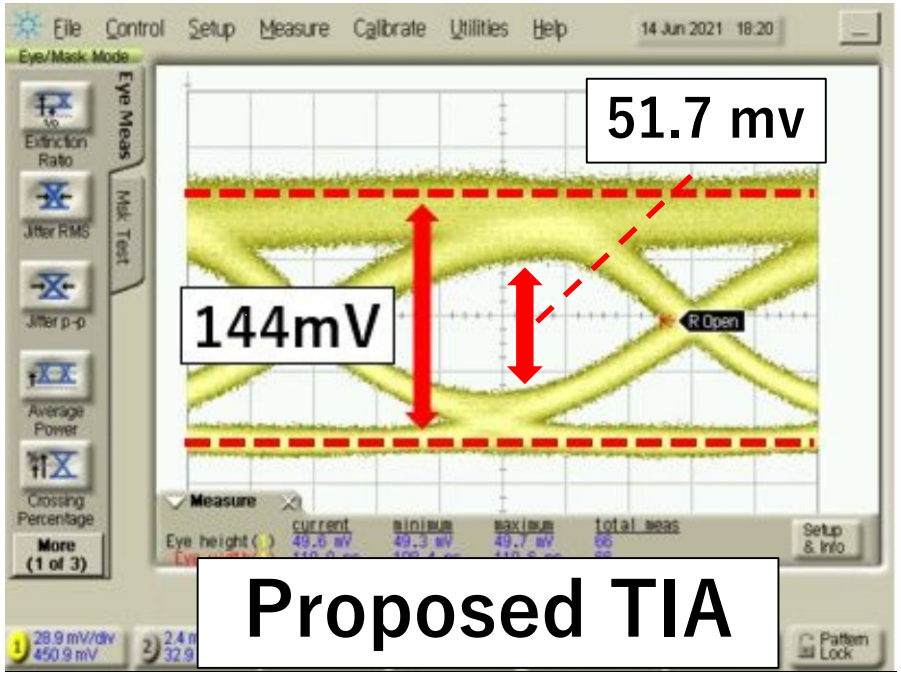
- Standard voltage is 1.8 V.
- TIA's power supply considers voltage drop by noise.
- TIA and BUF power supplies are separated.



Measure the effect of TIA supply voltage drop on the eye diagram.

Measurement result





Amplitude (Low level-Hi level) : Improved 2 times
Eye-opening voltage : Improved 3 times

Proposed TIA is good eye diagram.

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Conclusion

Our key idea :

- Combining the non-inverting and the inverting amplifier circuits.
- Cancel the effect of power supply variation.

- 180-nm CMOS process
- On-wafer probing
- TIA's supply voltage drops to1.5 V from 1.8 V.
- Input signal is 7.5 Gbps PRBS.

Measurement result :

- Amplitude (Low level-Hi level) : Improved 2 times
- Eye-opening voltage : Improved 3 times

Thank you for listening