Common-Centroid Layout for Active and Passive Devices: A Review and the Road Ahead

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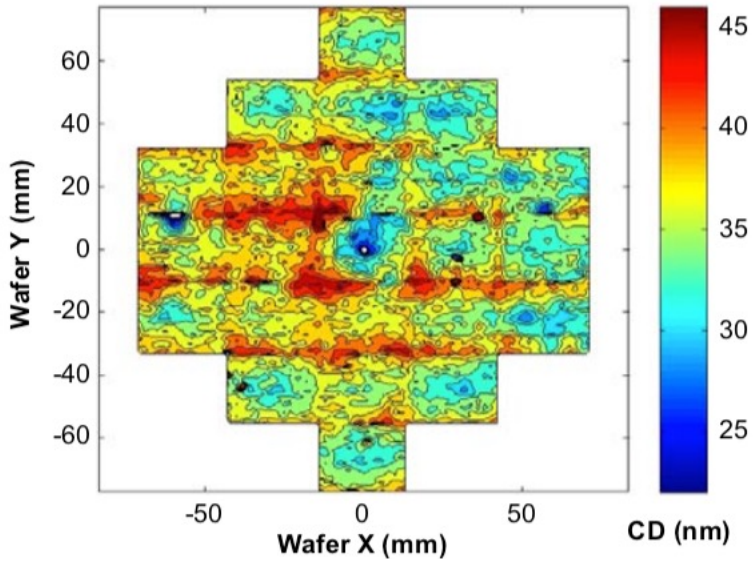
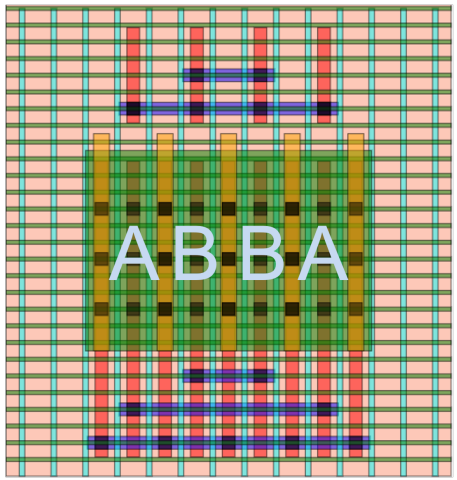
Background

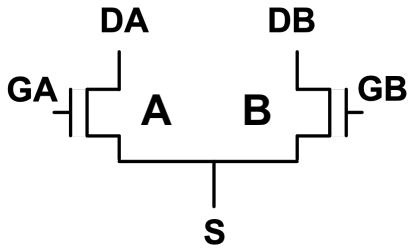
- Analog circuits
  - Often use large-sized devices/passives
    - Divided into unit structures laid out in an array
  - Sensitive to differential mismatch
    - Process variations are a major contributor



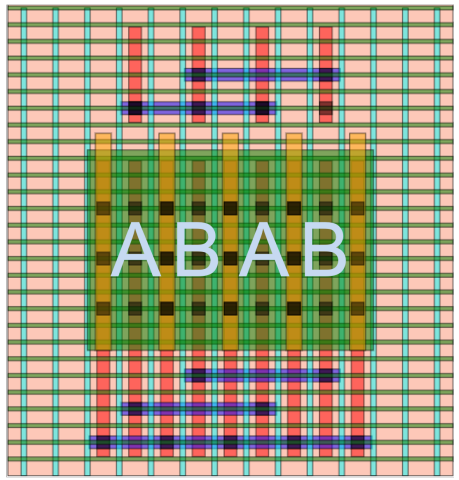
[Spanos, ISQED05]



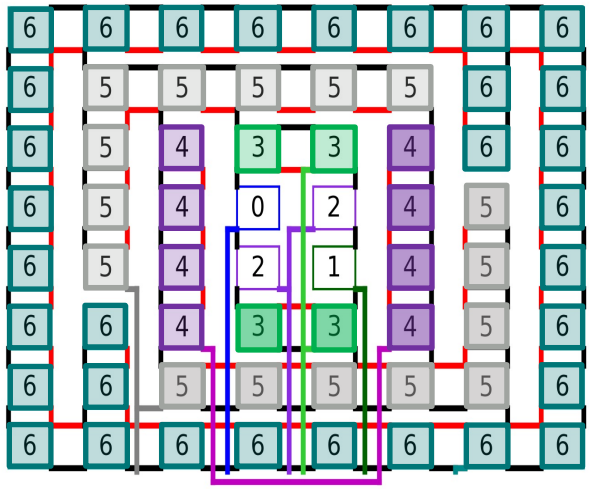
Common centroid



Differential pair
[Sharma, DATE21]

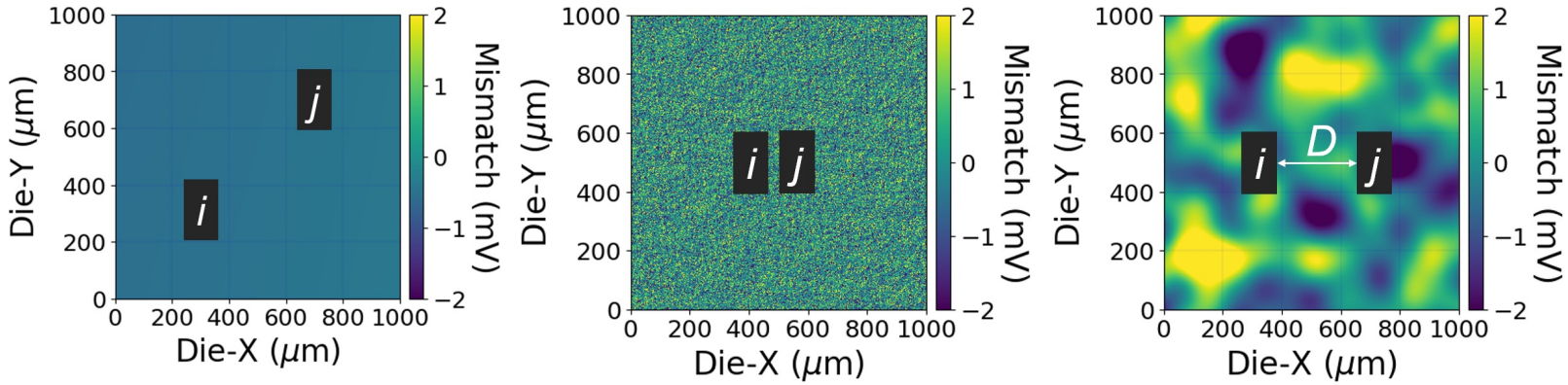


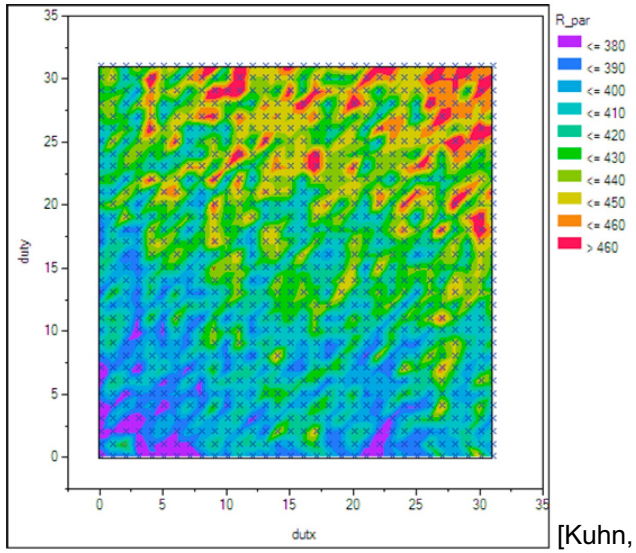
Interdigitated


[Karmokar, DATE22]

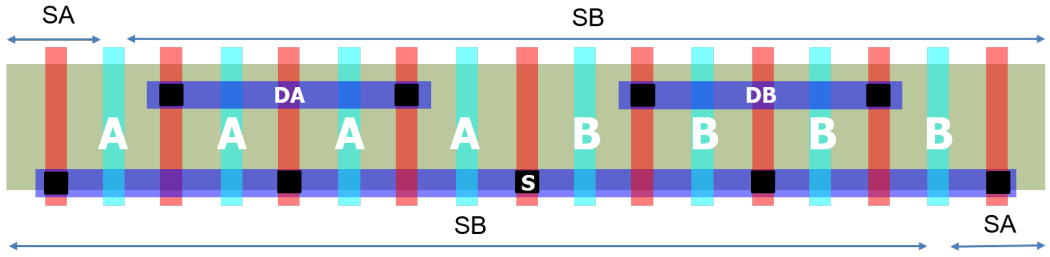
Variation Models

- Die-to-die variations
- Within-die random variations
  - Uncorrelated
  - Spatially correlated
- Systematic variations
  - Gradient variations
  - Layout-dependent effects (LDEs)

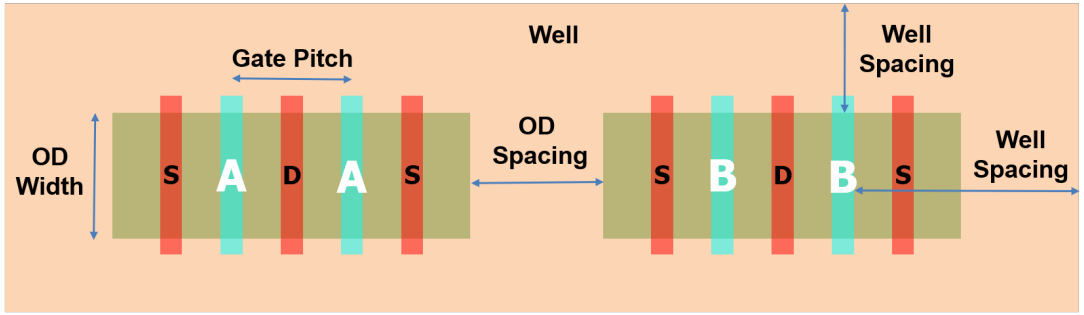




[Kuhn, 2010]



(a) SA and SB parameters for LOD effect.



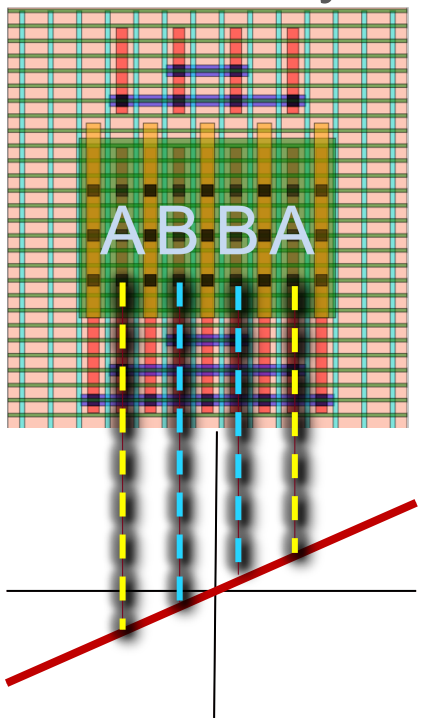
(b) OD width and spacing, gate pitch, and well proximity effects.
[Sharma, ICCAD21]

Common-Centroid Layout

- Set the centroid of unit cells of A to be the same as that of B

$$\frac{1}{s_A}\sum_{i=1}^{s_A} x_1^A = \frac{1}{s_B}\sum_{i=1}^{s_B} x_2^B$$

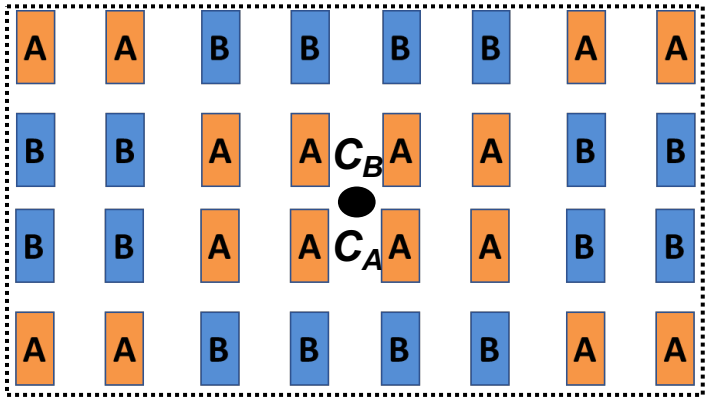
  - Can be extended to more devices
- Cancels out systematic process gradients



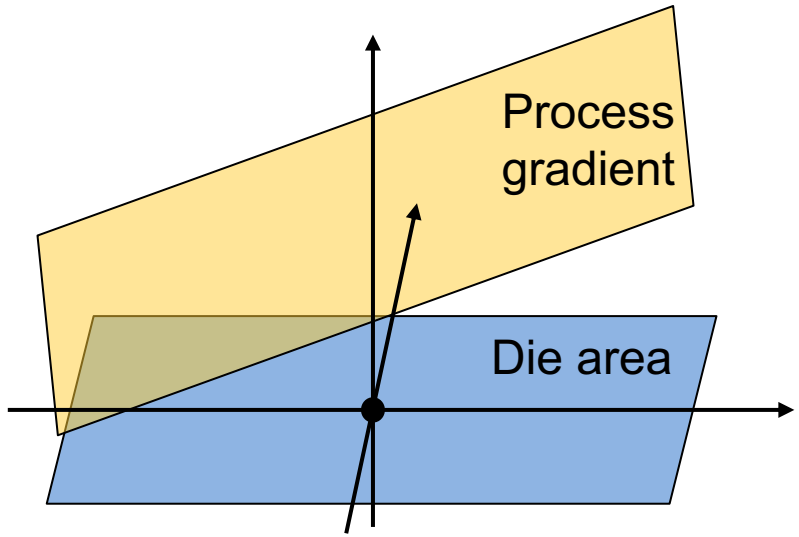
$$\Delta P = \mathcal{S}_p \Delta p$$

$$\Delta p = \alpha \cdot x$$

$$\Delta P = \alpha \mathcal{S}_p \cdot x$$

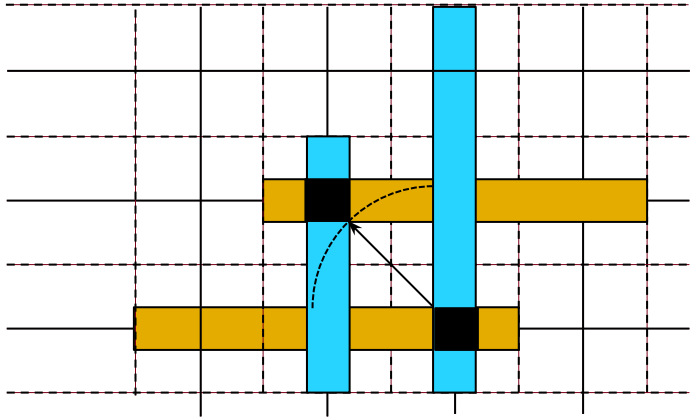


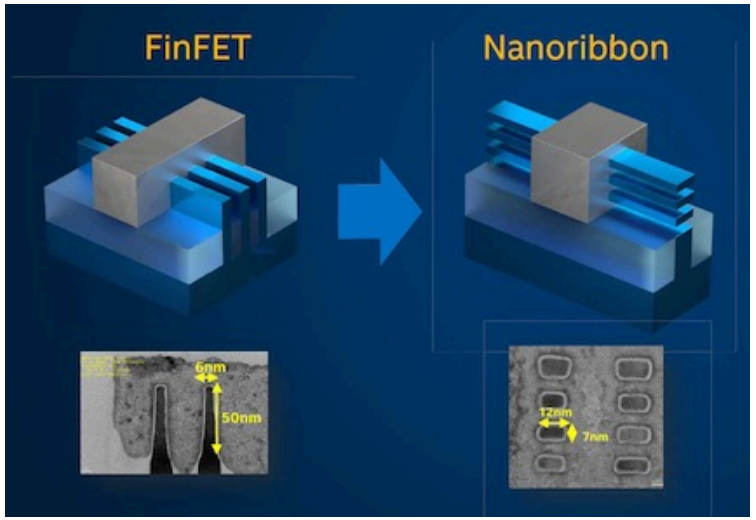
Common-centroid pattern



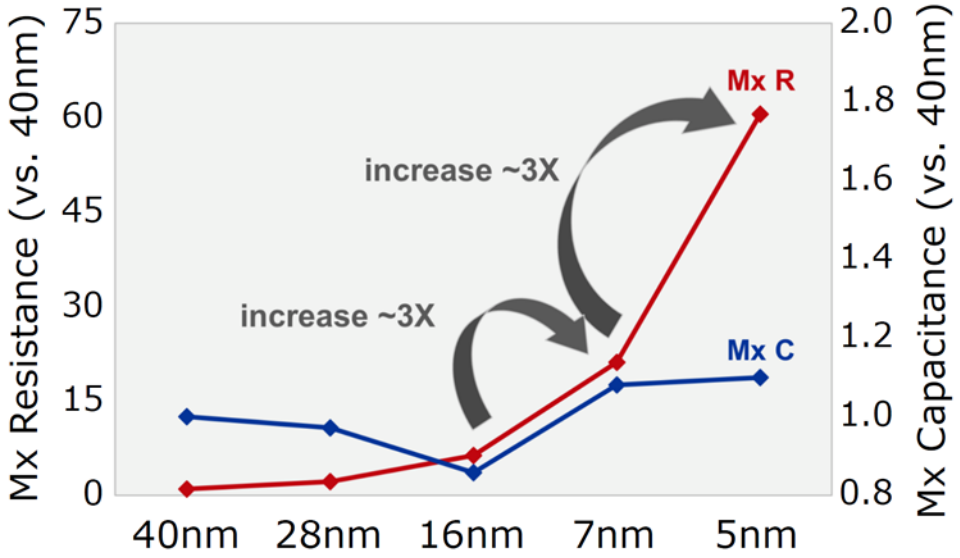
Trends in FinFET Technologies and Beyond

- High wire/via resistances
  - Bends discouraged
- Unidirectional transistors
- Gridded, unidirectional wires
- “Unit cells” for transistors
- Self-heating/electromigration issues





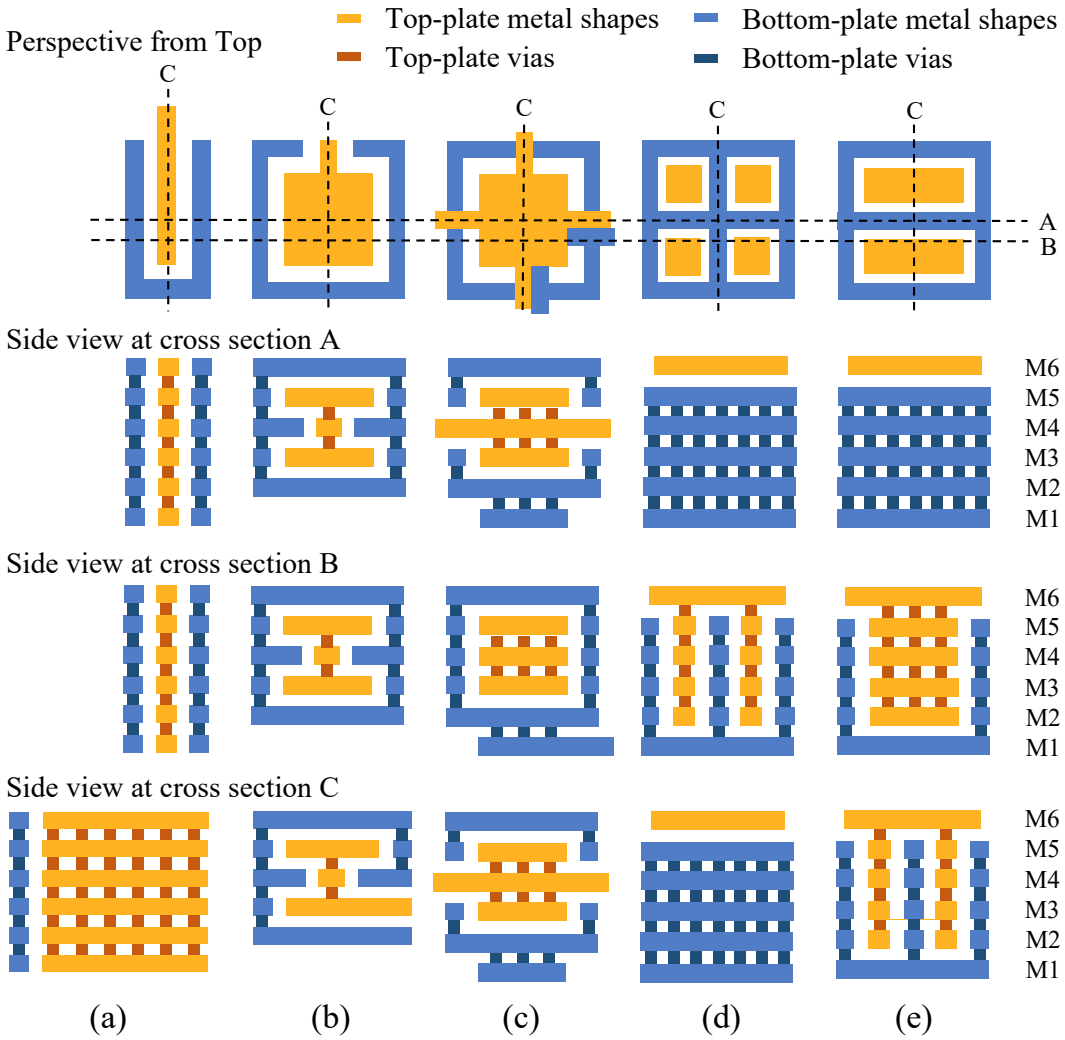
[anandtech.com]



[Hou, ISSCC2017]

Capacitor Layout

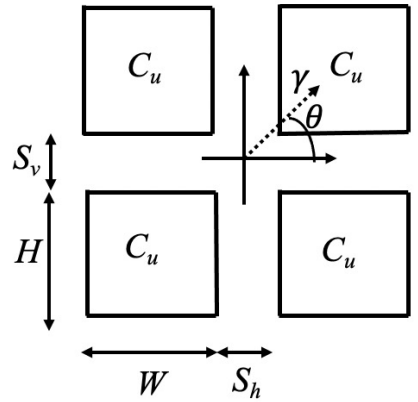
- Types of capacitors



[Wang, DAC20]

- Systematic mismatch

Process gradients



$$C_k^* = \sum_k C_u \frac{t_0}{t_k}$$

where $t_k = t_0 + \gamma(x_k \cos\theta + y_k \sin\theta)$

$$M_{sys} = \max_{p,q \in \{1,\cdots,n\}, p \neq q} \left| \frac{(C_p^*/C_q^*) - (C_p/C_q)}{(C_p/C_q)} \right|$$

Random Mismatch

- Correlation function

$$\rho_s(r) = (\rho_0)^r$$

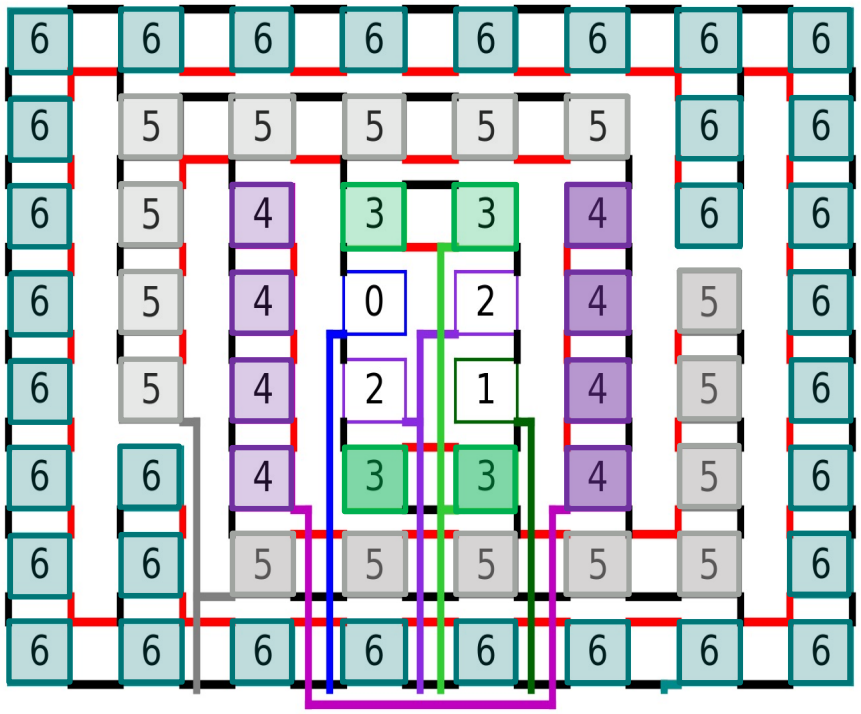
- For $C_p = p\ C_u$, $C_q = q\ C_u$

$$\rho_{pq} = \frac{Cov(p,q)}{\sigma_p \sigma_q}$$

- Metrics

$$\rho_{avg} = \frac{1}{C(t,2)} \sum_{p=1}^{t-1} \sum_{q=p+1}^{t} \rho_{pq}$$

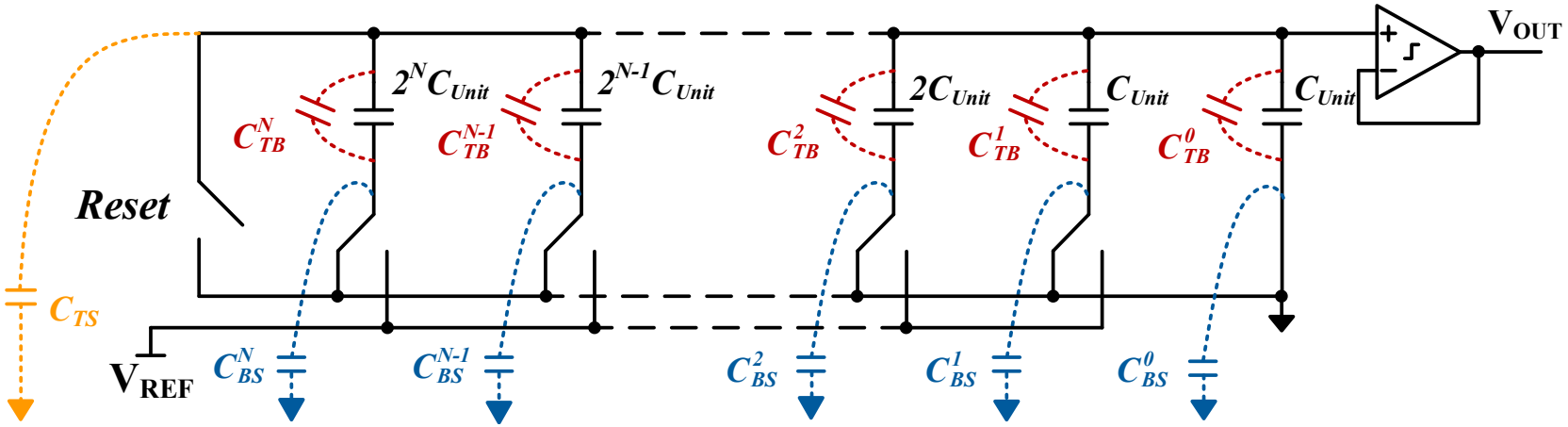
$$M_{rand} = \max_{p,q \in \{1,\cdots,n\}, p \neq q} var\left(\frac{C_p}{C_q}\right)$$



[Karmokar, DATE22]

Circuit Performance Metrics

- Charge-sharing DAC



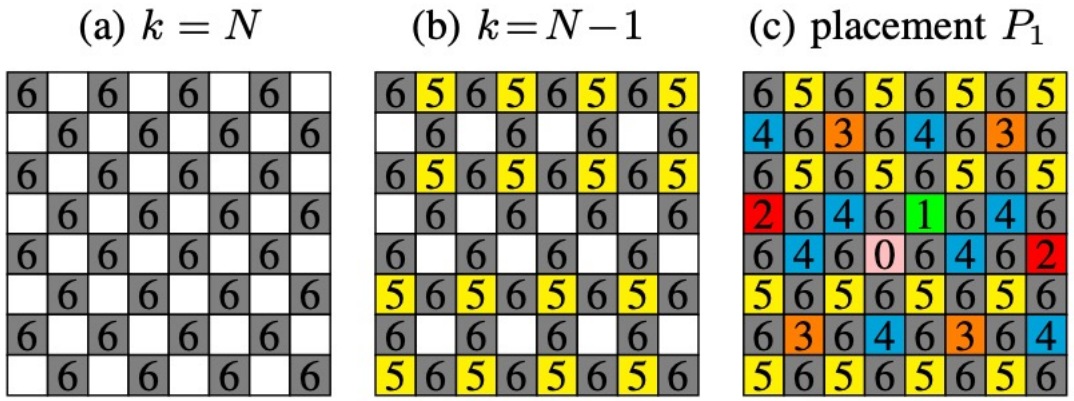
[Lin, TCAD17]

$$DNL_i = \frac{V_{OUT}(i+1) - V_{OUT}(i) - V_{LSB}}{V_{LSB}}, \forall i = 0, \ldots, 2^{N-1}.$$

$$INL_i = \frac{V_{OUT}(i) - V_{OUT}^{ideal}(i)}{V_{LSB}}, \forall i = 0, \ldots, 2^{N-1}.$$

CC Capacitor Layout Methods

- Heuristic
  - No guarantee of optimality (and sometimes correctness)
- ILP
  - Place unit capacitors and wires into “slots”
- Structured methods
  - Chessboard layout



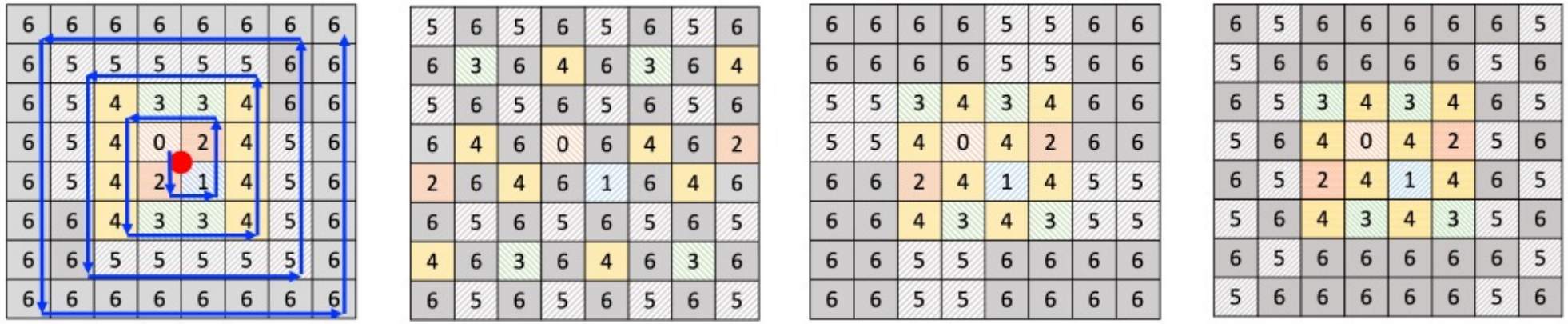
[Burcea, TCAD15]

- Iterative methods
  - Simulated annealing based perturbation of pair sequences with routability analysis

[Lin, TCAD17]

FinFET-based CC Capacitor Layouts

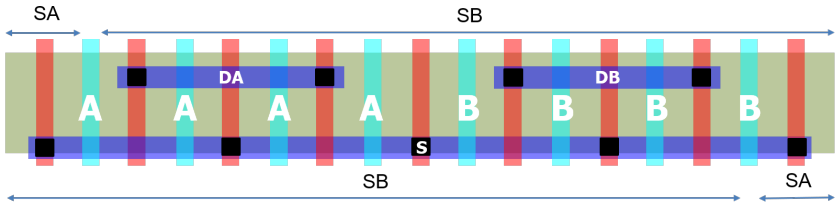
- High via counts lead to high resistance → high RC delays → low 3dB frequency
- Alternative layout styles that reduce via counts are preferred
  - Chessboard layouts achieve good dispersion, high via count
  - Block chessboard (BC) layouts achieve a good compromise



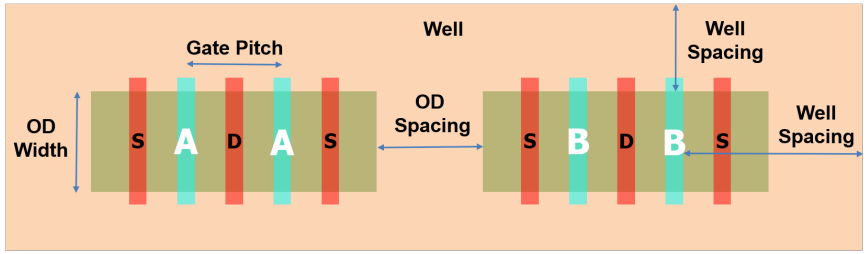
[Karmokar, DATE22]

Transistor Layout

- Layout-dependent effects (LDEs)



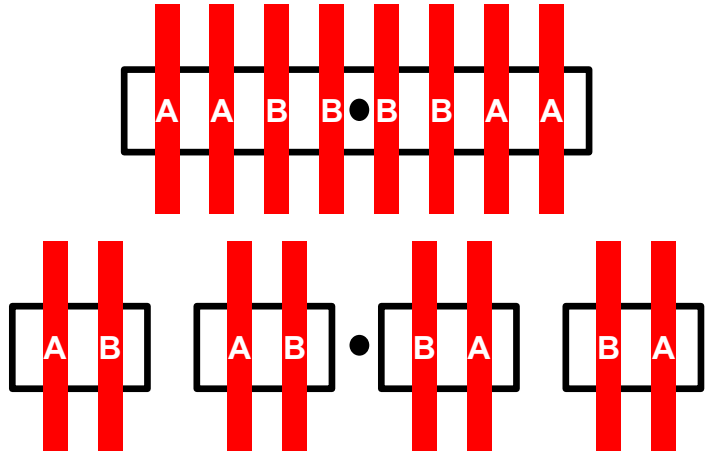
(a) SA and SB parameters for LOD effect.



(b) OD width and spacing, gate pitch, and well proximity effects.

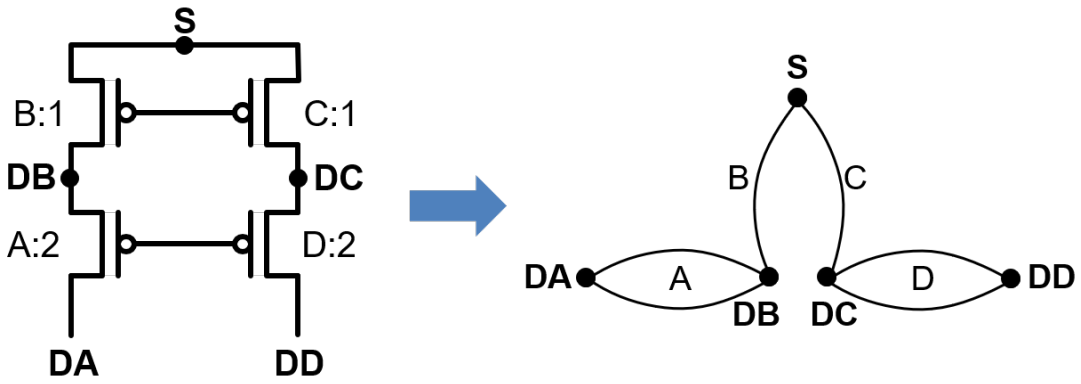
$$\Delta V_{th} \propto \frac{1}{\text{LOD}} = \sum_{i=1}^{n} \left(\frac{1}{\text{SA}_i + 0.5L_g} + \frac{1}{\text{SB}_i + 0.5L_g} \right)$$

- Diffusion sharing
  - Diffusion breaks require spaces, can create asymmetries



  - Transistor CC placement to maximize diffusion sharing

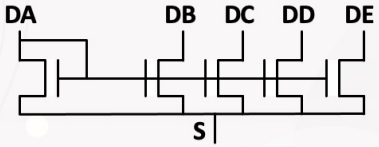
CC Transistor Placement



Input

M: [2, 2, 4, 8, 8]

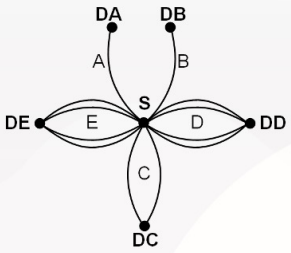
K = 1.3



Graph

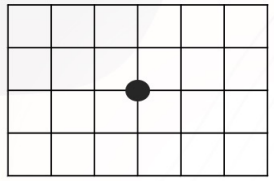
U: [0, 0, 0, 0, 0]

M_{half}: [1, 1, 2, 4, 4]

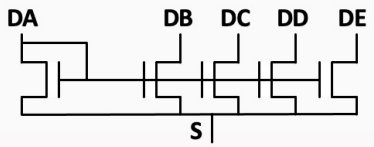


Aspect Ratio

Close to a square



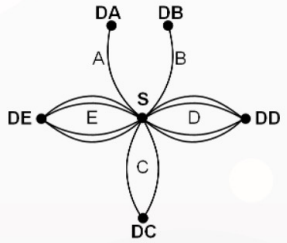
4 x 6



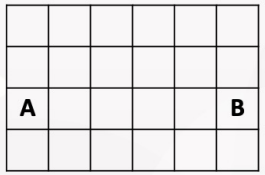
M: [2, 2, 4, 8, 8]

M_{half}: [1, 1, 2, 4, 4]

K = 1.3

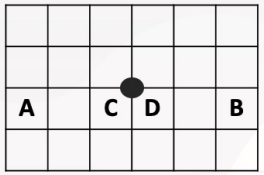


U: [0, 0, 0, 0, 0]



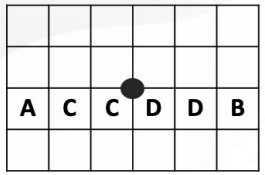
M_{temp}: [0, 0, 2, 4, 4]

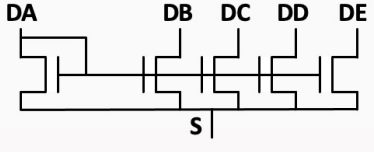
$Ratio$: [0, 0, 1, 1, 1]



M_{temp}: [0, 0, 1, 3, 4]

$Ratio$: [0, 0, 0.5, 0.75, 1]





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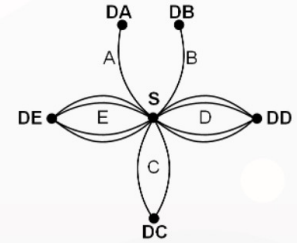
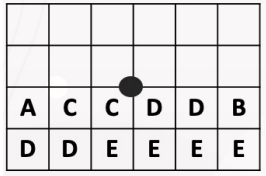
K = 1.3



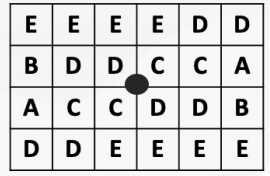
M_{temp}: [0, 0, 0, 0, 0]

$Ratio$: [0, 0, 0, 0, 0]

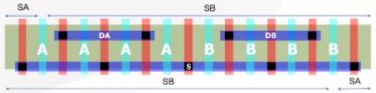


M_{temp}: [0, 0, 0, 0, 0]

$Ratio$: [0, 0, 0, 0, 0]



Postprocessing



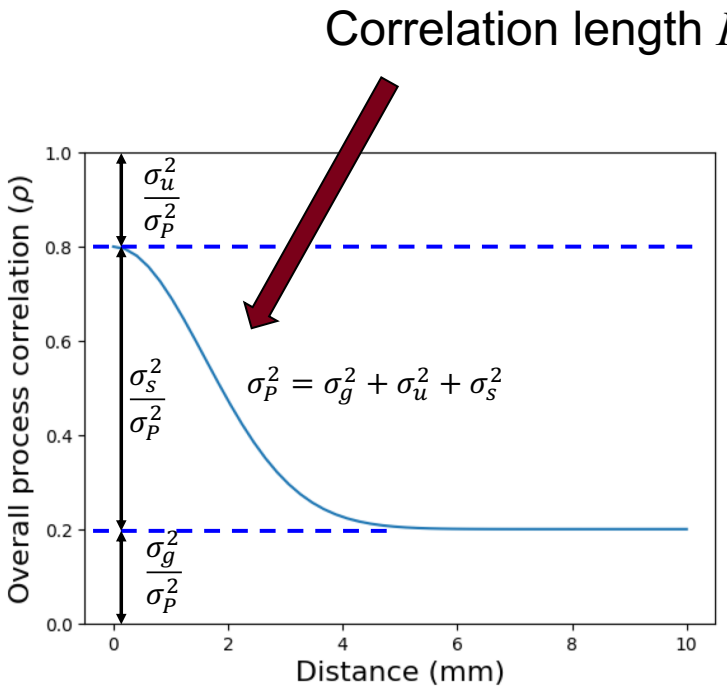
$$\Delta V_{th} \propto \frac{1}{\mathrm{LOD}} = \sum_{i=1}^{n} \left(\frac{1}{\mathrm{SA}_i + 0.5L_g} + \frac{1}{\mathrm{SB}_i + 0.5L_g} \right)$$

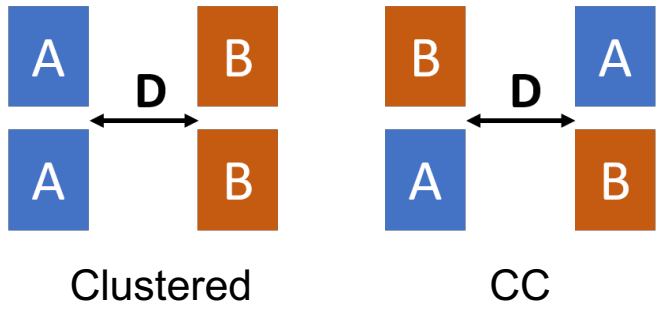
$$\Delta V_{th}^{max} \leq \varepsilon V_{th}$$

Placement is followed by EM-aware/IR-drop-aware routing

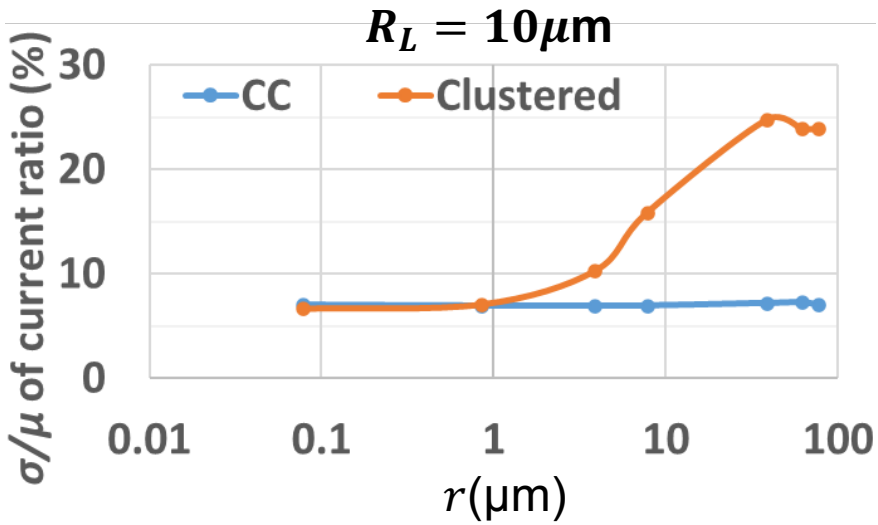
[Sharma, ICCAD21]

When is CC Layout (Un)necessary?





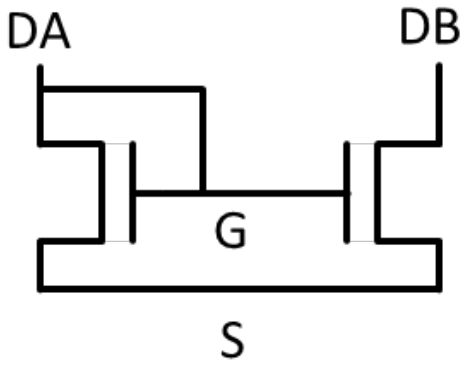
[Sharma, DATE21]



CC is not beneficial when layout size $\ll$ R_L

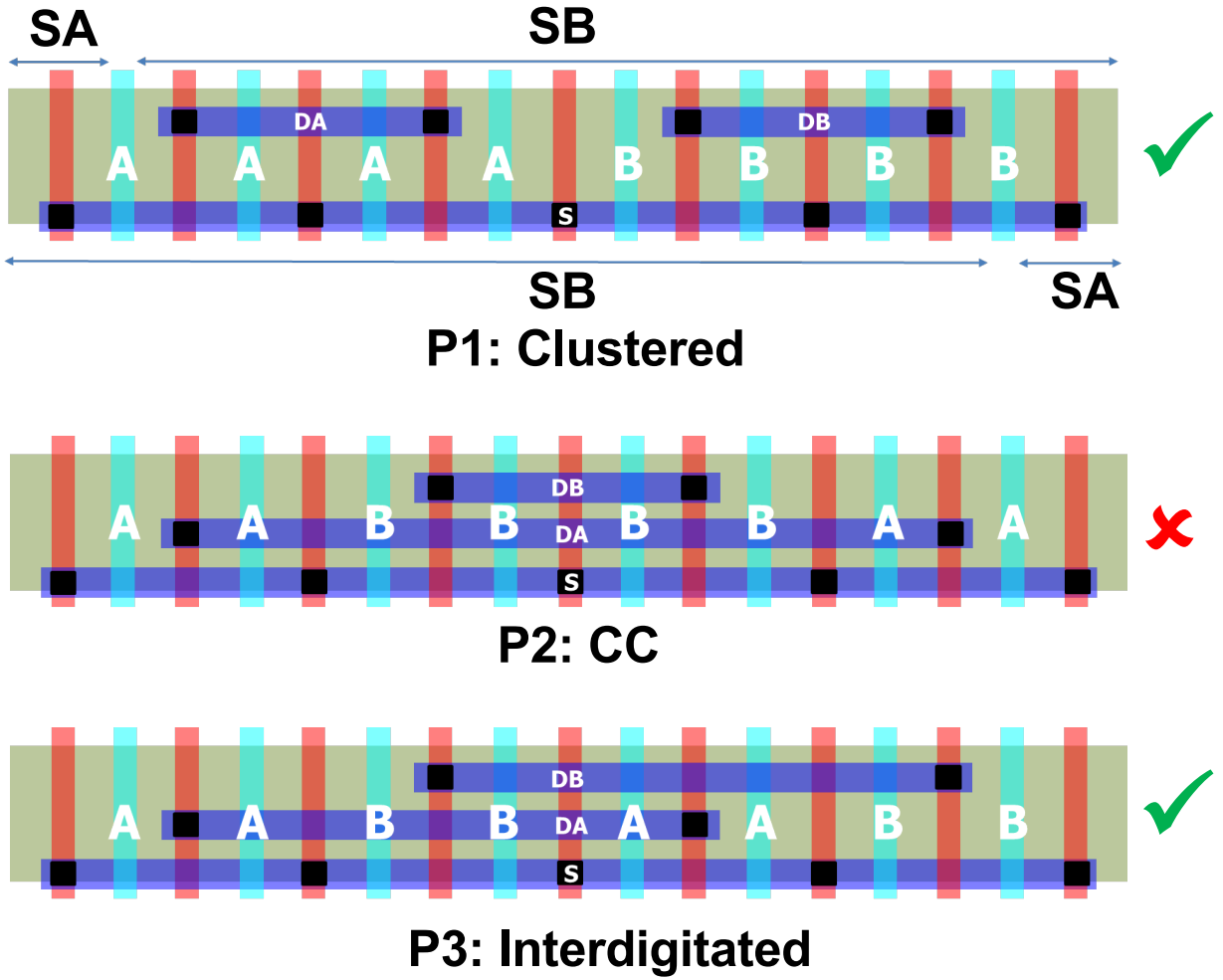
When is CC Layout (Un)necessary?

- LDEs affect the mean value: CC does not match LDEs



Current mirror

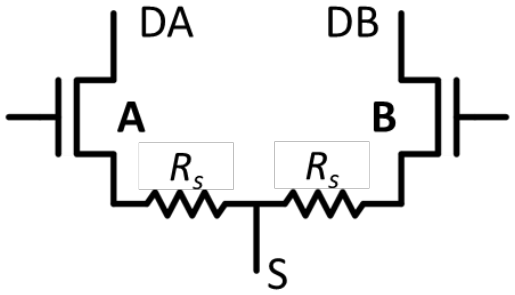
$$V_{th} \propto \frac{1}{\mathrm{LOD}} = \sum_{i=1}^{n} \left(\frac{1}{\mathrm{SA}_i + 0.5L_g} + \frac{1}{\mathrm{SB}_i + 0.5L_g} \right)$$

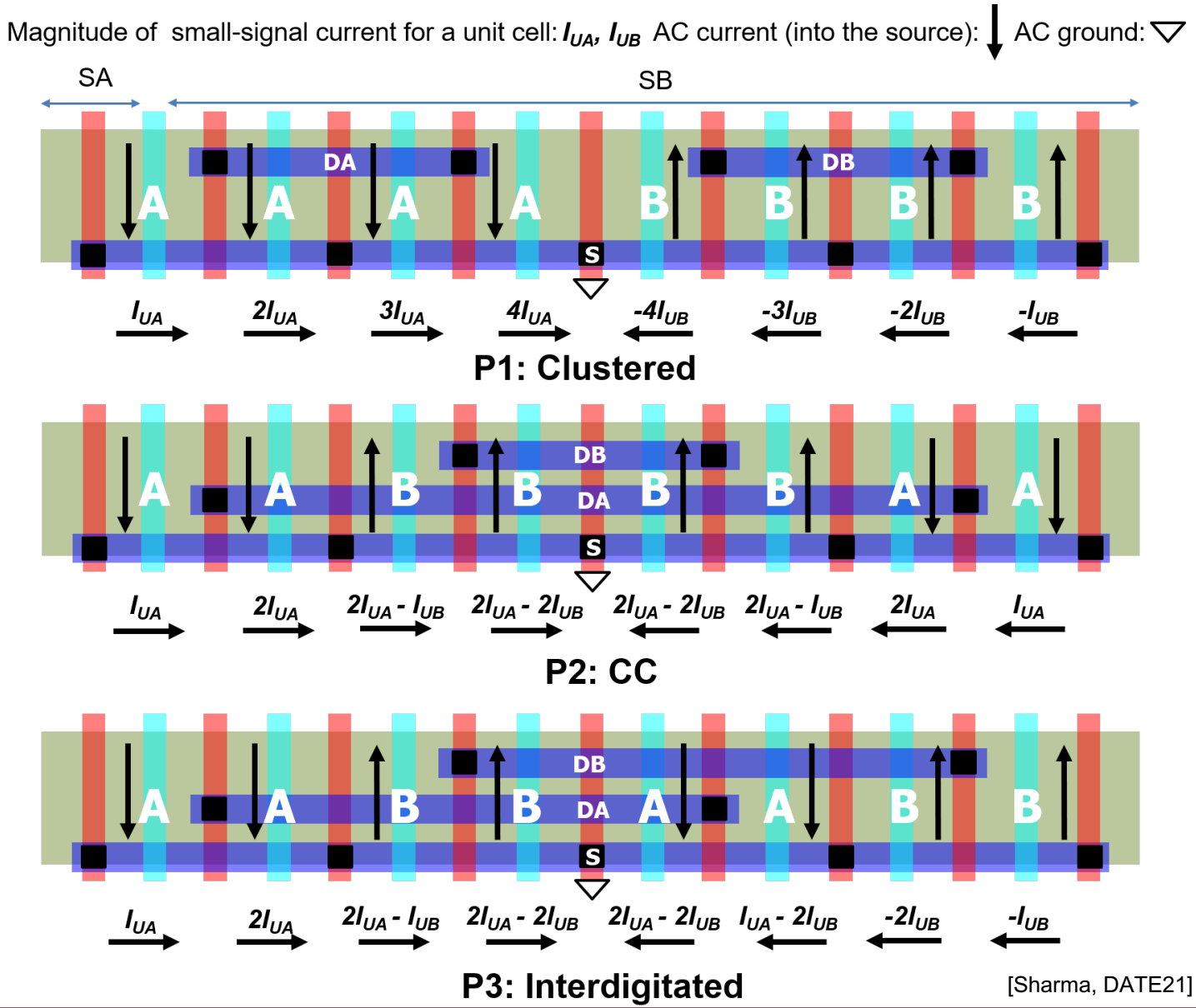


[Sharma, DATE21]

When is CC Layout (Un)necessary?

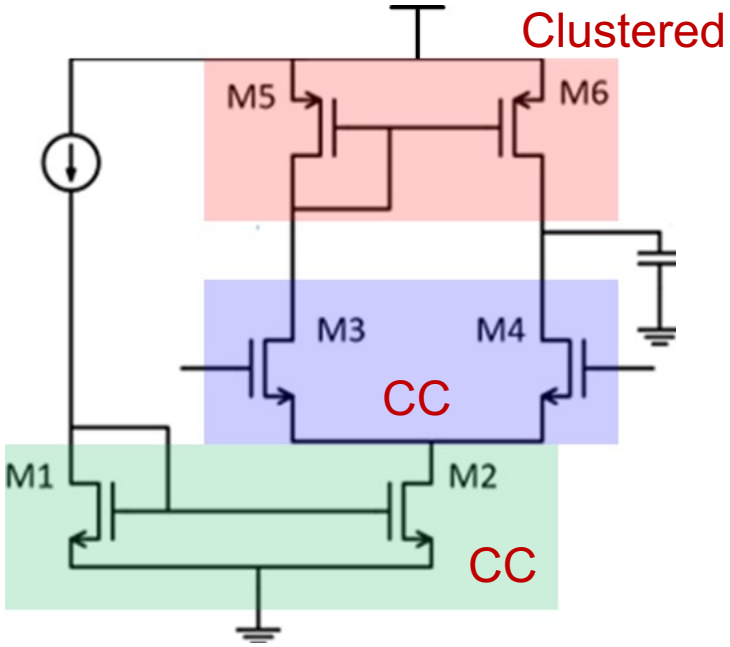
- Impact of parasitics

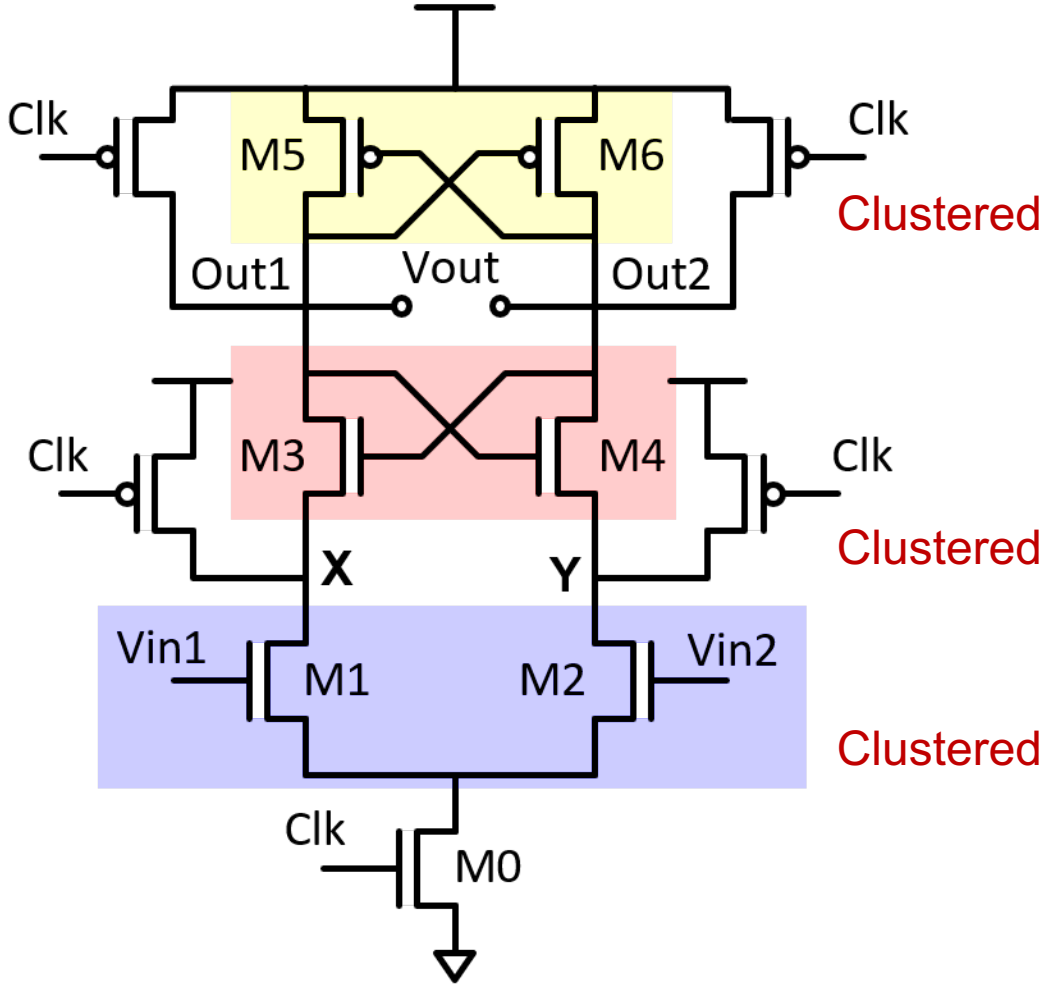




[Sharma, DATE21]

Optimal Layouts May Differ from Block to Block





[Sharma, DATE21]

Conclusion

- CC layout is important in canceling systematic variations
- CC layout styles for transistor and passive arrays are widely used
- In FinFET technologies
  - Must be aware of correlation lengths
  - Must be aware of wire/via resistances
  - Avoid diffusion breaks
  - Consider alternatives to CC due to LDEs, wire parasitics, layout size