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Signal-Integrity-Aware Interposer Bus Routing in 2.5D Heterogeneous Integration

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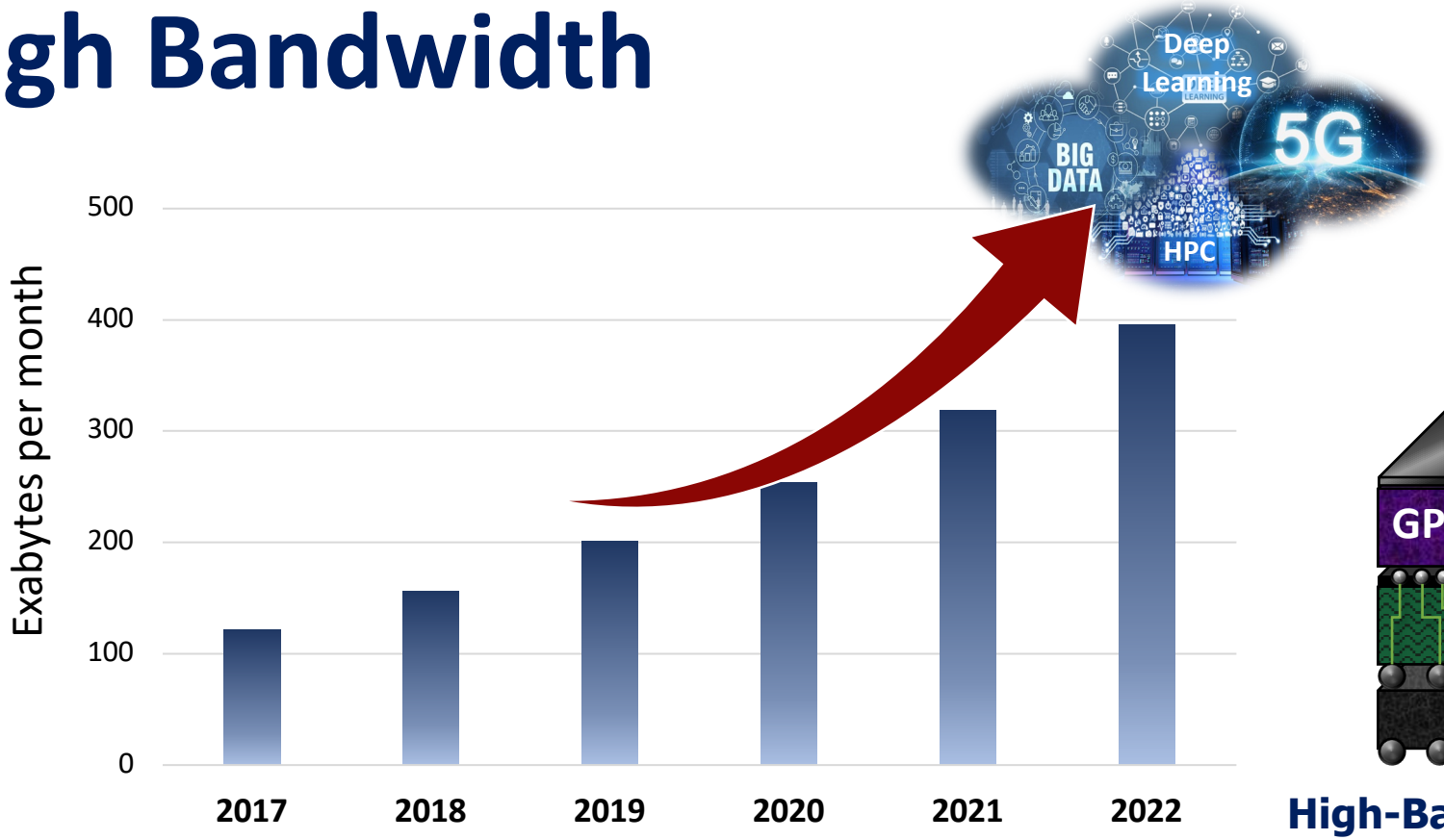
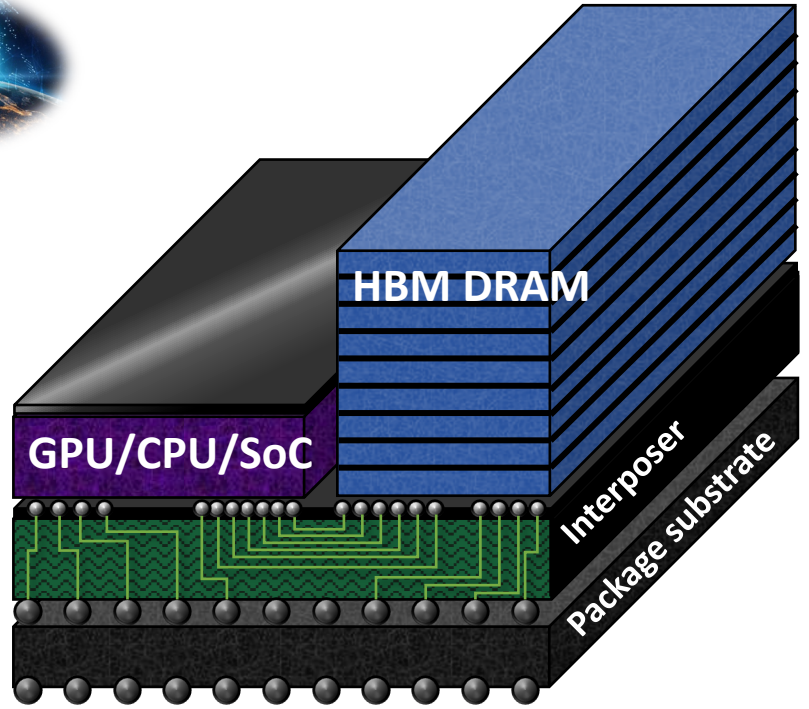
High Bandwidth



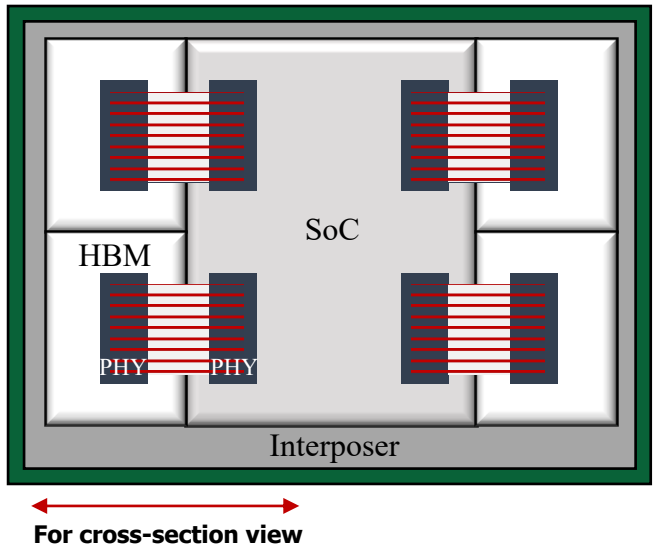


High-Bandwidth Memory (HBM) in 2.5D IC

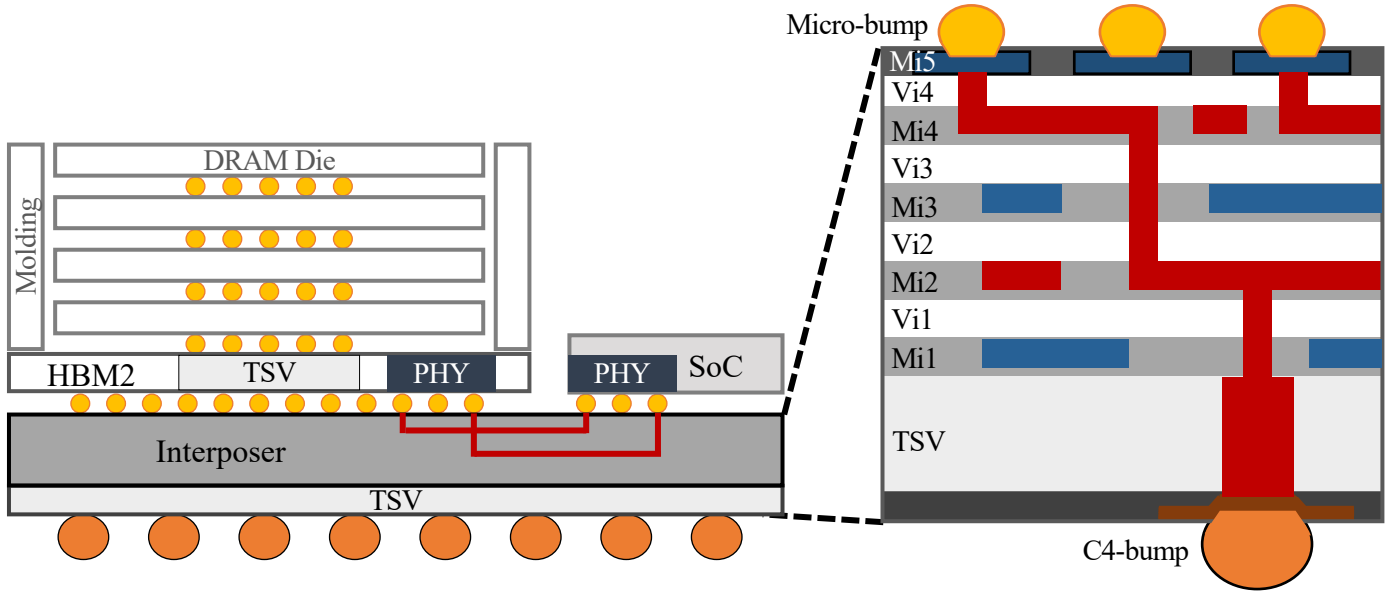
- Demands on high bandwidth are exponentially increasing.
- High bandwidth memories (HBMs) are integrated in 2.5D ICs.

Silicon Interposer Layer

Top view of a 2.5D IC

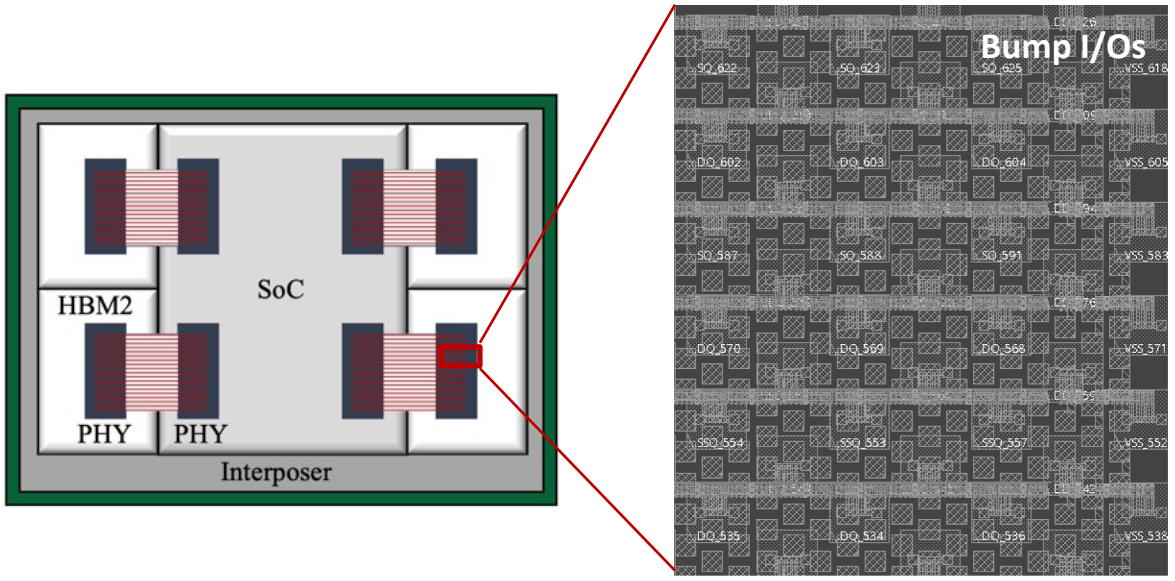


Cross-section view of a 2.5D IC



- Interposer layer is used for interconnection between chiplets.
- For high bandwidth, thousands of channels transmit data at high speed.
- Interpose channels are vulnerable to crosstalk and data loss.

Interposer Routing



Complicating factors for routing

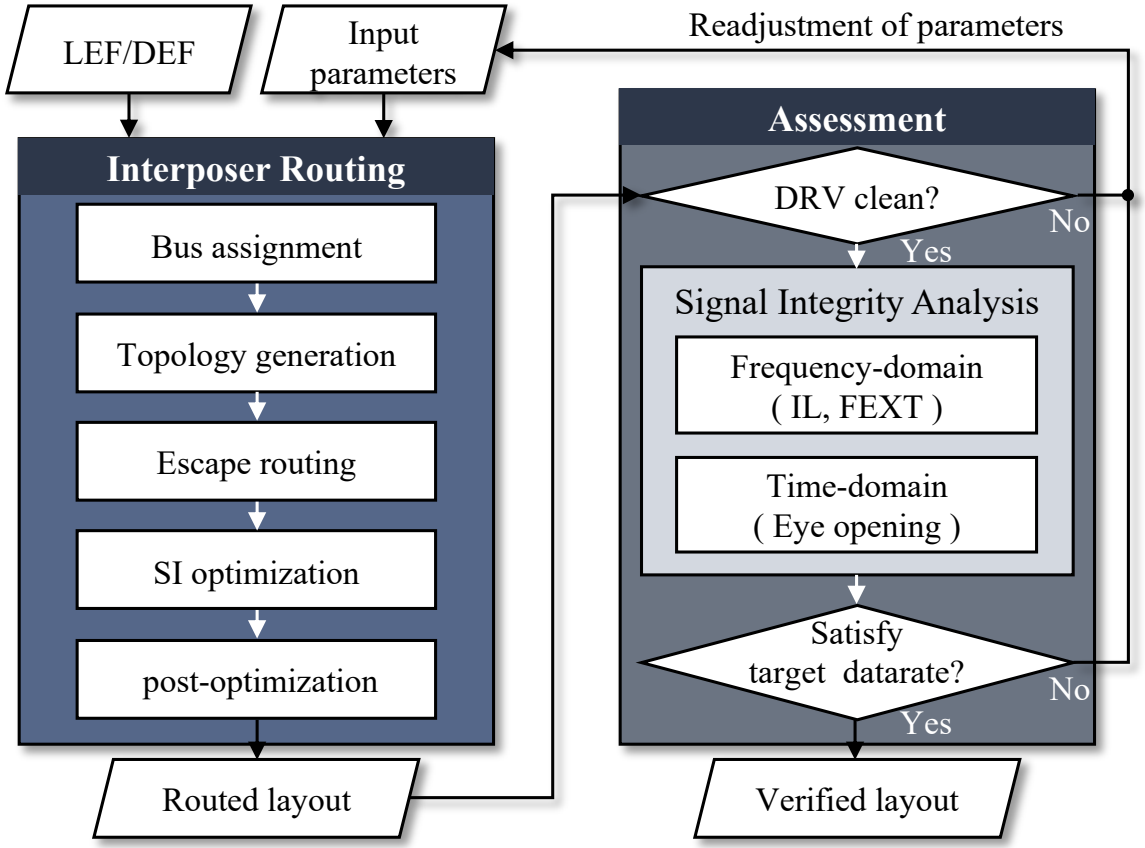
- Limited number of interposer layers
- Increasing number of bump I/Os
- Various bump patterns & tech node
- Geometric offsets between chiplets
- Complex design rules
- Metal guarding for signal integrity
- Wirelength matching for zero-skew

- Traditional manual routing takes too much time and effort of designers.
- **Fast & tech-independent interposer auto-router becomes essential.**

Interposer Bus Routing

Interposer Bus Routing

- **Overall flow**



Inputs

- **Netlist**
- **Bump I/O placed layout**

Outputs

- **Routed layout**

Objectives

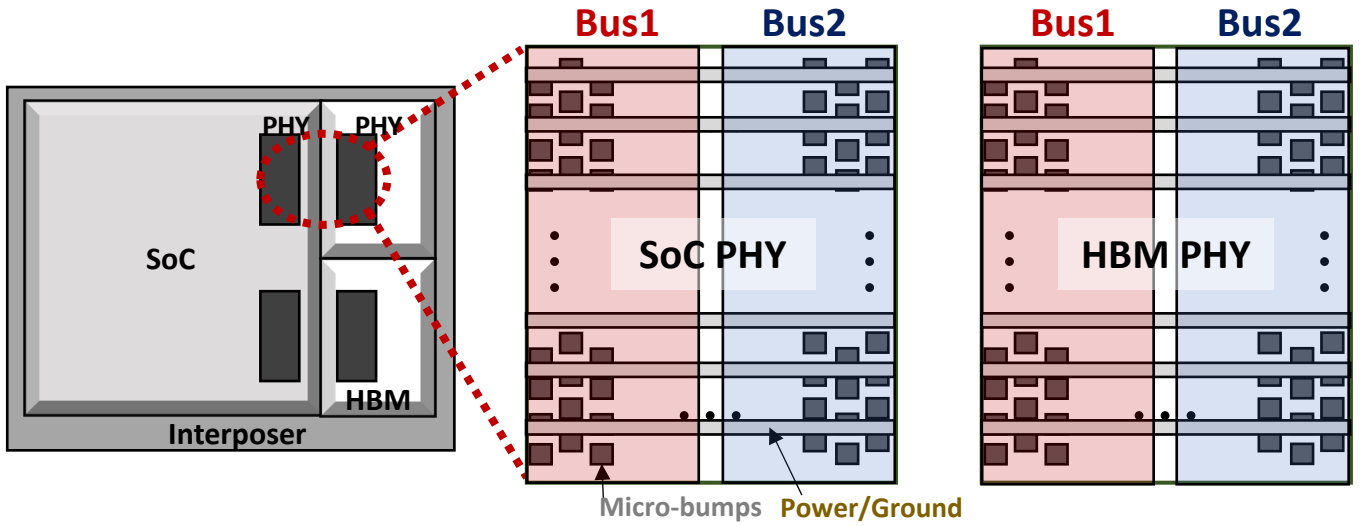
- **Maximize signal integrity**

Constraints

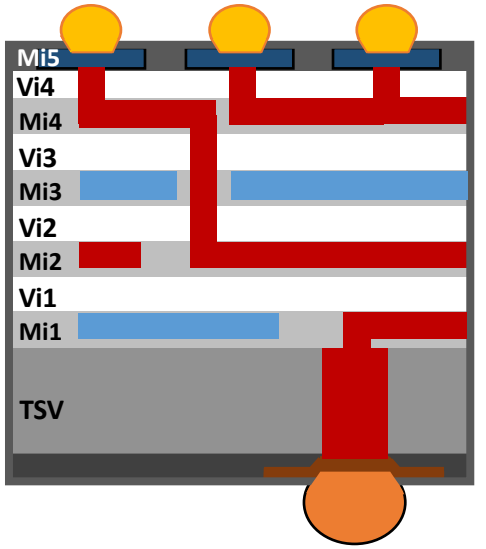
- **Design rules**
- **Wirelength matching**

Bus & Layer Assignment

Bus assignment



Layer assignment



Mi5: Bump I/O placement

Mi4: Bus1 routing

Mi3: Metal guarding

Mi2: Bus2 routing

Mi1: Power routing

Microstrip-like structure for routing layers

Objectives

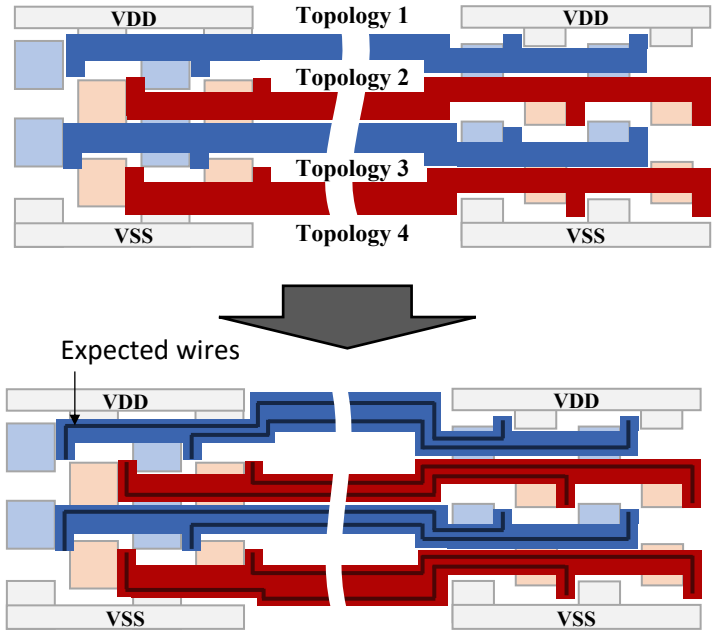
- Maximize routing resource
- Simplify wirelength matching problem

Restrictions

- Bump patterns
- VDD/VSS power line

Escape Routing

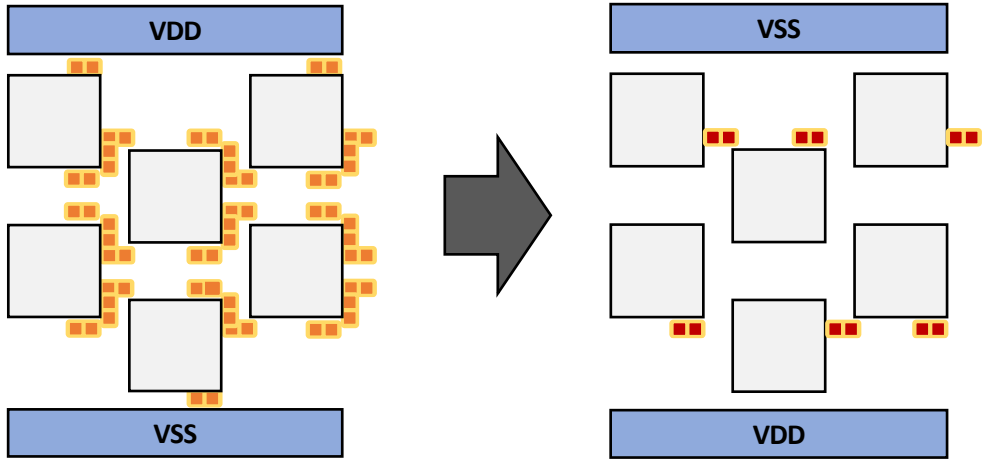
1. Topology generation



2. Via placement

Minimize resource error

- Intervals between vias or VDD/VSS
- Required resources by following topology



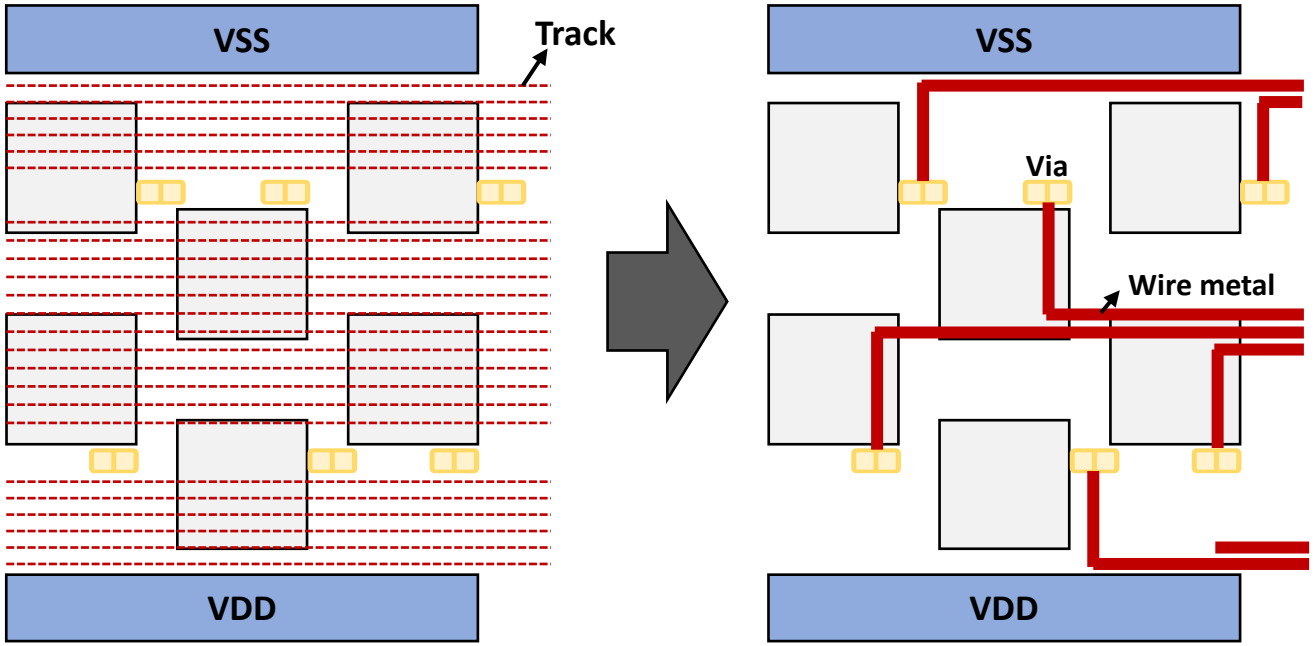
Candidates of via location

Placed via

- Hook-shaped topology is a common topology to avoid short violations.
- To maximize wire pitch, our router firstly places vias, then assigns wires to tracks.

Escape Routing

3. Track assignment



Bump ordering

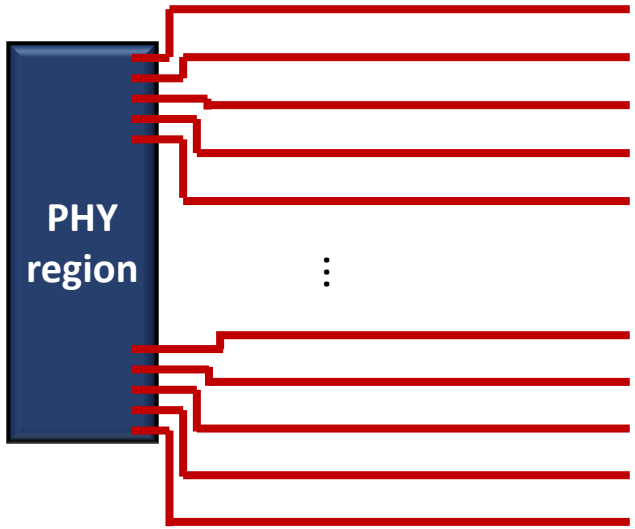
$$order(m,l) = \#col \times \left\lceil \frac{m}{2} \right\rceil + (-1)^{m+k} \times \left\lfloor \frac{l \bmod (\#col)}{2} \right\rfloor + (m+k+1) \bmod 2$$

- Bump is placed at m-th row and l-th column
- #col: the number of columns of bumps in the same bus
- k: the number of rows of bumps between VDD/VSS.

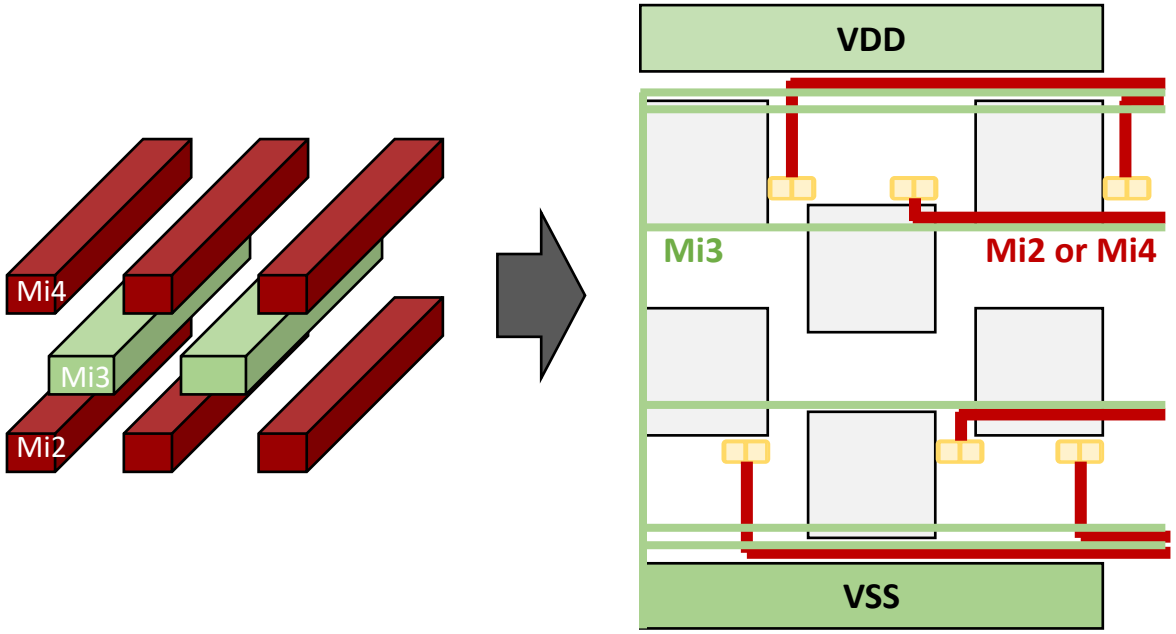
- **Assign tracks with observing design rules including spacing, width, area rules.**
- **To follow the topology, tracks are assigned in the order of bumps.**

Signal Integrity Optimization

1. Widen pitch in non-PHY region



2. Metal guarding



- Narrow and long parallel wires are critical to signal integrity
- Widening wire pitch and guarding signal wires improves signal integrity.

Experimental Results

Experimental Setup

- **Silicon interposer specifications**

Parameter	Value
Thickness of routing layers	1 μm
Thickness of cut layers	1 μm
Dielectric constant of SiO_2	4
Loss tangent of SiO_2	0
Conductivity of Al	3.8×10^7 S/m
Conductivity of Cu	5.8×10^7 S/m

- **Benchmark specifications**

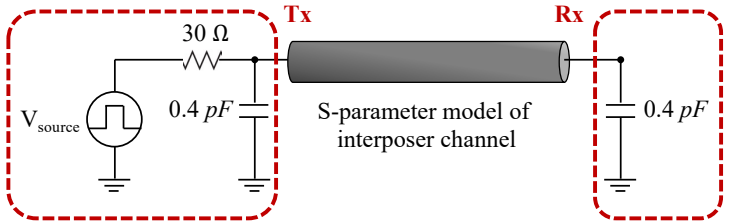
Bench	*Testcase 1*	*Testcase 2*
Number of nets	3496	
Area of SoC PHY	14.25 mm^2	
Area of HBM2 PHY	19.28 mm^2	
Area of non-PHY region	19.80 mm^2	40.20 mm^2
Offset between PHYs	0 mm	3.23 mm
X-pitch of micro-bumps	96 μm	
Y-pitch of micro-bumps	55 μm	
Number of bump-rows btw. VDD/VSS	4	
Target bandwidth per I/O pin	3.2 *Gbps*	

Router

- Implemented in C++
- Linux 2.3-GHz CPUs and 8 threads

Signal integrity analysis

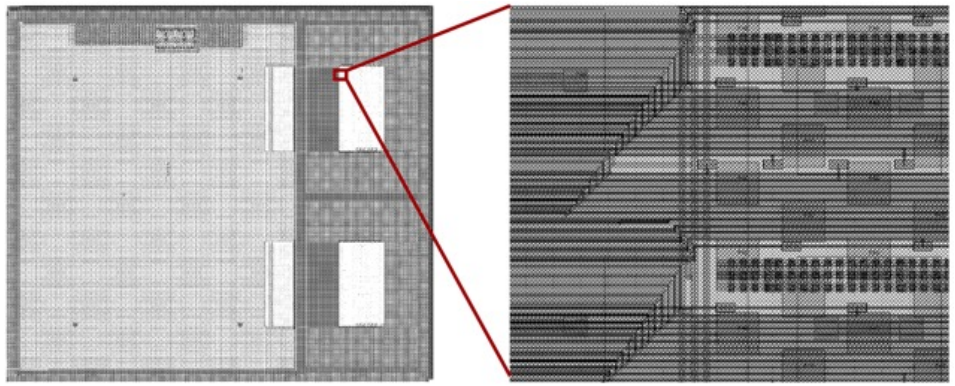
- ANSYS siwave, aedt circuit design
- Modeling transceiver and receiver



Voltage swing [*V*]	0 – 1.2
Target datarate [*Gbps*]	3.2 (1 *UI* = 312.5 *ps*)
Rising/falling time [*ps*]	45
Phase delay [*ps*]	0
PRBS length	15

Experimental Results

- **Routed Layout (*Testcase1*)**



- **Design parameters**

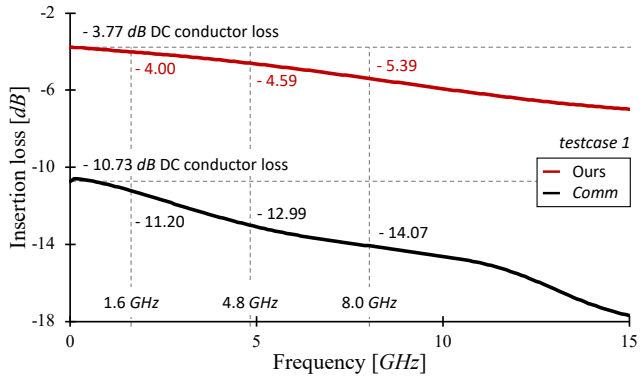
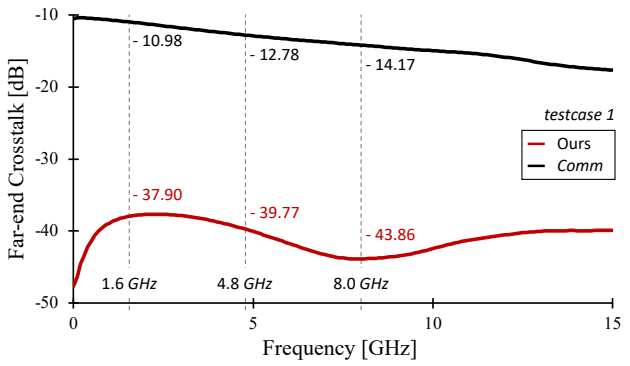
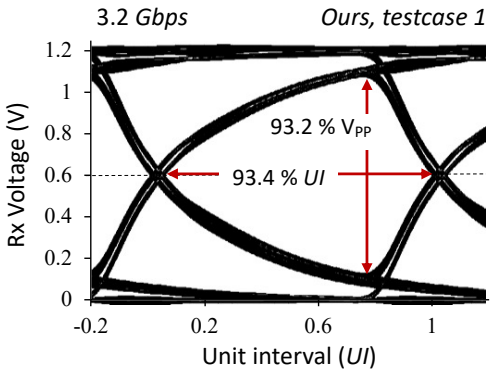
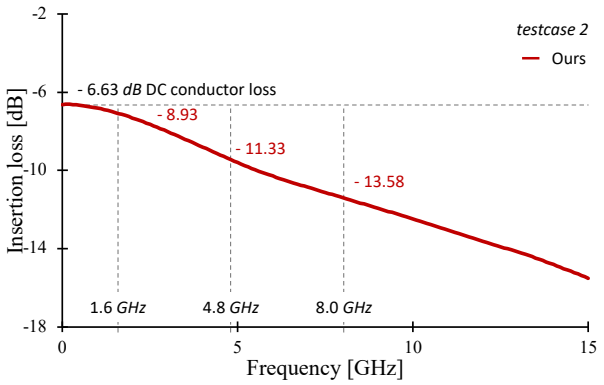
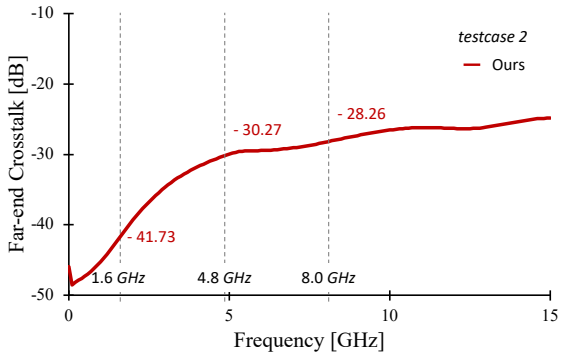
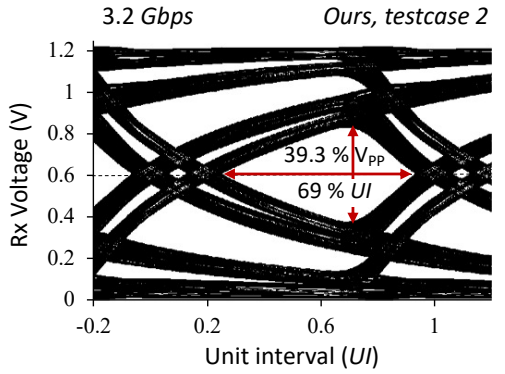
Bench	Router	Width [μm]	Min. pitch [μm]	Guard width [μm]
Testcase1	*Comm*	1.50	4.00	-
	Ours	1.52	4.77	3.00
Testcase2	*Comm*	1.50	4.00	-
	Ours	1.45	4.62	2.75

- **Routing quality**

Bench	***Testcase1***		***Testcase2***	
Router	*Comm*	Ours	*Comm*	Ours
Avg. WL [μm]	4948	4655	9125	9067
Max. WL_{diff} [μm]	1858	14	2536	291
Mi5 usage [%]	0.34	0.03	9.16	0.02
#_vias	26876	6984	32568	6984
#_DRVs	1108	0	2185	0
Runtime[s]	1250	199	1334	227

- **Our router shortened average wirelength.**
- **Our router matched wirelength with only ~1% error.**
- **Our router used 80% less vias.**
- **Our router resulted no design rule violations.**
- **Our router is ~5 times faster.**

Signal Integrity Results

	Insertion loss	Far-end crosstalk	Eye-diagram
Testcase1			
Testcase2			

Operating frequency: 1.6 GHz

CONCLUSION

Conclusion

Summary

- We propose an interposer router that interconnects heterogeneously integrated chiplets with different tech nodes and bump patterns.
- Our router achieves much better results than commercial SW in respect to routing quality, signal integrity, and runtime.

Future work

- Diagonal routing with various angles to further shorten wirelength.
- Find the optimal design parameters using machine learning.

THANK YOU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