

Net Separation-Oriented Printed Circuit Board Placement via Margin Maximization

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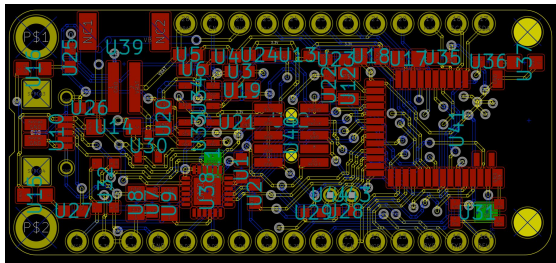


UC San Diego

Overview

- ▶ Printed Circuit Board Placement
- ▶ NS-Place: motivation, construction, formulation
- ▶ Experiments
- ▶ Conclusion

Printed Circuit Board (PCB) Placement

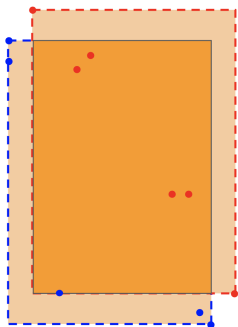


- ▶ Printed circuit board (PCB) placement as a benchmark for the packaging problem.
 - ▶ Multiple placement and routing layers
 - ▶ Arbitrary component sizes, shapes, and rotations
 - ▶ High utilization

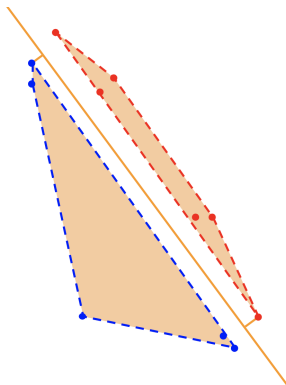
Contributions

- ▶ Existing methods for congestion are *pessimistic*.
- ▶ We propose NS-Place for PCB layout: minimizes net congestion using SVMs and an *optimistic* congestion model.
- ▶ Formulates legalization as a congestion-aware MILP
- ▶ Variable and constraint pruning via (relative position) constraint substitution

An Optimistic Model of Congestion¹



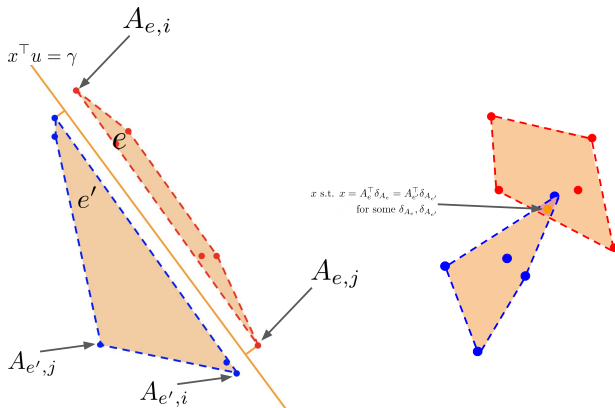
classic congestion modeling



our model

¹Spindler & Johannes, Fast and Accurate Routing Demand Estimation for Efficient Routability-driven Placement, DATE'07

Convex Hull Construction



net	$e \in \mathcal{E}$
pin matrices	A_e
convex hull coefficients	u, γ

Formulation

$$\begin{aligned} &\exists \delta_{A_e} \in \mathbb{R}^k, \delta_{A_{e'}} \in \mathbb{R}^{k'} \\ &\text{such that } A_e^T \delta_{A_e} = A_{e'}^T \delta_{A_{e'}}, \quad \mathbf{1}^T \delta_{A_e}, \mathbf{1}^T \delta_{A_{e'}} = 1, \\ &\quad \delta_{A_e}, \delta_{A_{e'}} \geq 0 \end{aligned}$$

Formulation

$$\begin{aligned} \exists \delta_{A_e} \in \mathbb{R}^k, \delta_{A_{e'}} \in \mathbb{R}^{k'} \\ \text{such that } A_e^T \delta_{A_e} = A_{e'}^T \delta_{A_{e'}}, \quad \mathbf{1}^T \delta_{A_e}, \mathbf{1}^T \delta_{A_{e'}} = 1, \\ \delta_{A_e}, \delta_{A_{e'}} \geq 0 \end{aligned}$$

Duality & Farkas' Lemma: conditions must be satisfied if the convex hulls *do not* intersect:

$$\begin{aligned} A_e u \geq \alpha \mathbf{1} \quad A_{e'} u \leq \beta \mathbf{1} \quad \alpha - \beta > 0 \\ \implies A_e u - \gamma \mathbf{1} \geq \mathbf{1}, \quad A_{e'} u - \gamma \mathbf{1} \leq -\mathbf{1} \end{aligned}$$

Minimizing Congestion

$$\begin{aligned} 0 &= \min_{u, \gamma} f(e, e', u, \gamma) \\ &= \min_{u, \gamma} \left(\|(-A_e u + (\gamma + 1)\mathbf{1})_+\|_2 + \right. \\ &\quad \left. \|(A_{e'} u - (\gamma - 1)\mathbf{1})_+\|_2 \right) \end{aligned}$$

Let A_e be the pin matrix corresponding to net e . We define the net-separation regularizer (over all nets) to be

$$Ns(\cdot) = \frac{1}{|\mathcal{M}|} \sum_{e' \in \mathcal{E}} \min_{u, \gamma} f(e, e', u, \gamma)$$

Minimizing Congestion

Our framework implies a *Bi-level* optimization problem for placement:

$$\min_{x,y} \sum_{e \in \mathcal{E}} [W_a(e; x, y) + \lambda_{NS} N_s(e; x, y)] + \lambda_D D(x, y)$$

Generally NP-Hard (especially since D is non-convex).

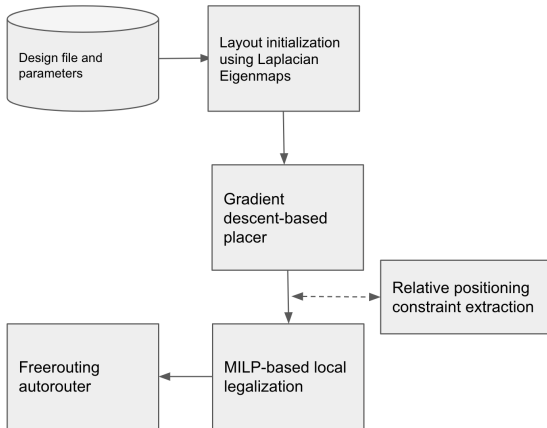
Minimizing Congestion

We can reach a local solution:

1. We can solve for μ, γ using off-the-shelf SVM solvers.

2. Update x, y with gradient descent

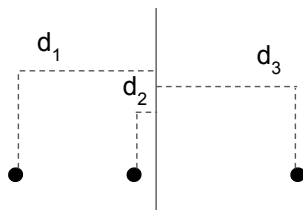
Placement Flow



Flow: Initialization

$$\begin{aligned} \min \quad & x^T Lx + y^T Ly \\ \text{s.t.} \quad & v^T x = 0, \quad v^T y = 0, \quad x, y \neq 0 \\ & x^T Dx = c_1, \quad y^T Dy = c_2, \quad x^T Dy = c_3 \end{aligned}$$

1. Objective: minimize the squared wire length
2. Linear constraints: concentrate the layout about the origin and prevent the trivial solution
3. Quadratic constraints: spread the placement over the axes.



1-d example of constraints.

Flow: Legalizataion

$$\min_{x,y,r} \left[\sum_{i \in |\mathcal{E}|} \text{hpwl}(i) + \left[\max_{i \in |\mathcal{E}|} \text{hpwl}(i) - \min_{i \in |\mathcal{E}|} \text{hpwl}(i) \right] \right]$$

$$\text{hpwl}_x(i) = (U_x^{(i)} - L_x^{(i)})$$

Flow: Legalizataion

$$\min_{x,y,r} \left[\sum_{i \in \mathcal{E}} \text{hpwl}(i) + \left[\max_{i \in \mathcal{E}} \text{hpwl}(i) - \min_{i \in \mathcal{E}} \text{hpwl}(i) \right] \right]$$

$$\text{hpwl}_x(i) = (U_x^{(i)} - L_x^{(i)})$$

where the *horizontal* HPWL and relative position constraints are given by

$$U_x^{(i)} \geq p_j^{(i)}(x), \quad L_x^{(i)} \leq p_j^{(i)}(x) \quad \forall j \in \mathcal{E}_i$$

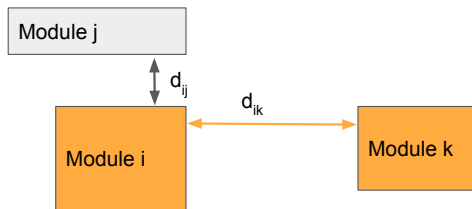
$$x_i + r_i h_i + (1 - r_i) w_i \leq W \quad \text{width}$$

$$x_i + r_i h_i + (1 - r_i) w_i \leq x_j + W(p_{ij} + q_{ij}) \quad \text{i-left-j}$$

$$x_i - r_j h_j - (1 - r_j) w_j \geq x_j - W(1 - p_{ij} + q_{ij}) \quad \text{i-right-j}$$

$$x_i, y_i \geq 0, \quad r_i, q_{ij}, p_{ij} \in \{0, 1\}$$

Relative Position Constraints

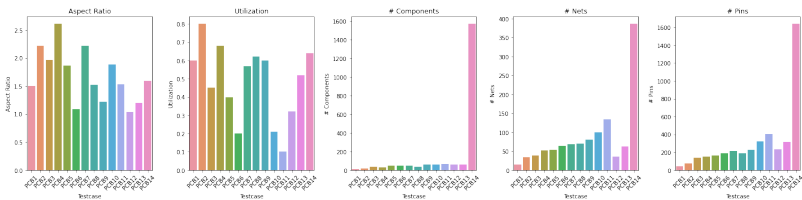


Add relative position constraint if $d_{ik} > d_{ij}$ and $d_{ik} > k$:

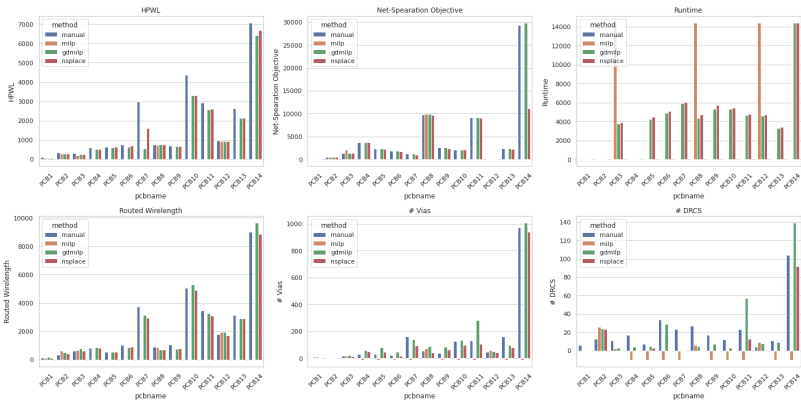
1. Prune variables p_{ik} , q_{ik}
2. Replace four constraints with a single constraint:

$$x_k - r_i h_i - (1 - r_i) w_i \geq x_i$$

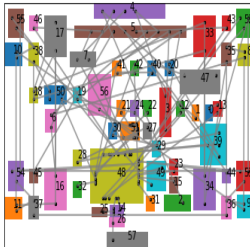
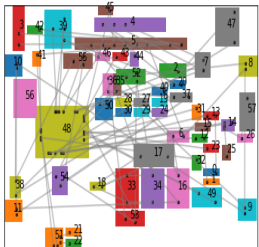
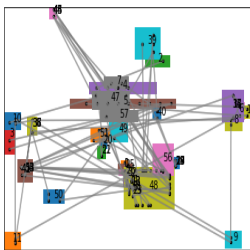
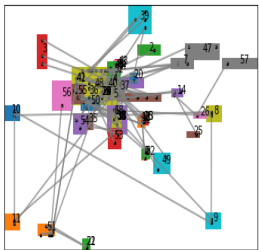
PCB Benchmark Suite



Quantitative Results



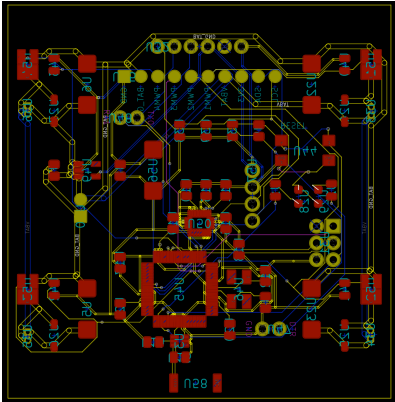
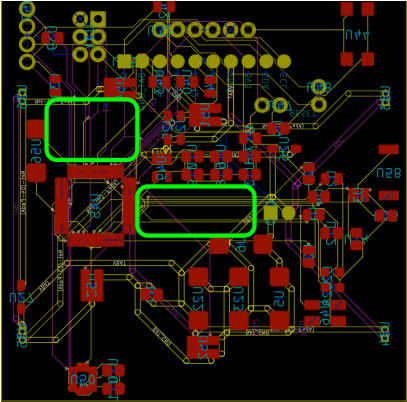
Qualitative Results



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Net Separation via Margin Maximization

Qualitative Results



Conclusion and Future Work

- ▶ We have presented a novel algorithm which encourages routability of multi-pin nets in PCB designs.
- ▶ We perform an extensive study on 14 PCB designs
- ▶ 80.98%, 70.00%, and 74.68% reduction on average #DRVs and #unrouted nets for routability
- ▶ 34.36% fewer #Vias on average
- ▶ Investigating nonlinear separators, better initialization and optimization strategies