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A Fast and Accurate Middle End of Line Parasitic Capacitance Extraction for MOSFET and FINFET Technologies Using Machine Learning

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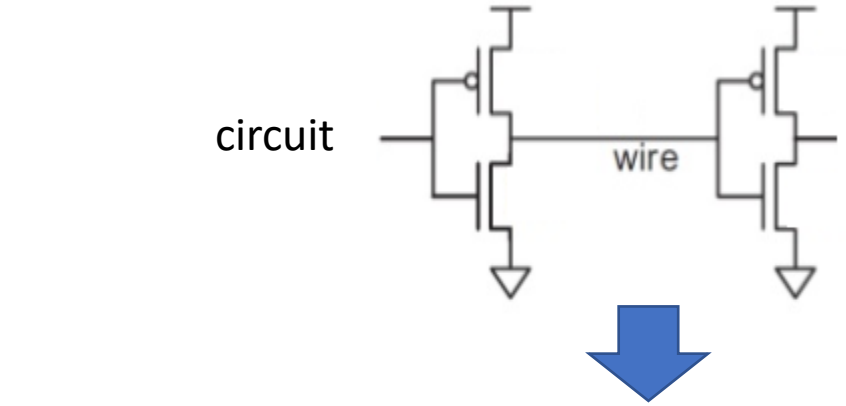
Agenda

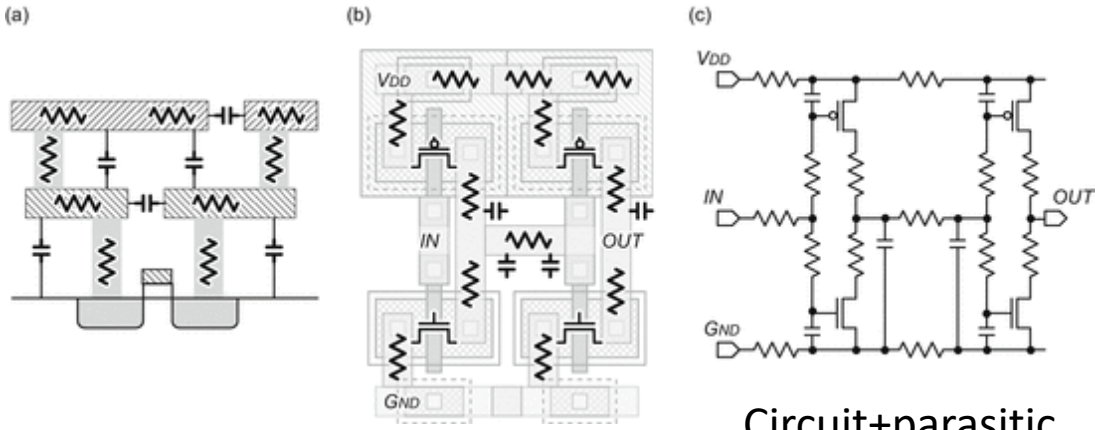
- Parasitic extraction…why?
- Parasitic capacitance extraction methods.
- Middle End of Line (MEOL)
- Rule-based Parasitic Extraction.
- Problem Definition.
- Machine learning Models.
  - Data preparation
  - Input representation (feature extraction)
  - Model’s creation
- Experimental results.

Parasitic extraction…why?

- In ICs, parasitic devices are the capacitors, resistors, and inductors that aren't included in the original circuit design but exist due to the non-ideal nature of the interconnect wires.

- The parasitic devices cause/impact:
  - Extra power consumption.
  - Delay.
  - Noise margin (can cause logic failures).
  - Increase IR Drop (on the power supply).
  - Increase signal noise.
  - Power distribution.



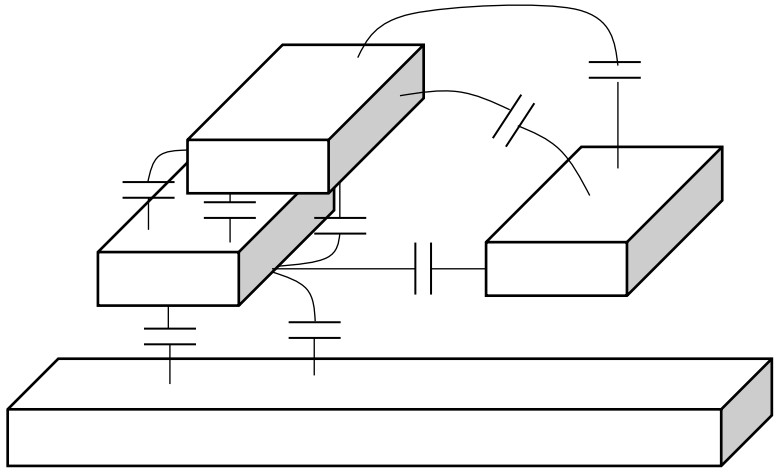


Circuit+parasitic

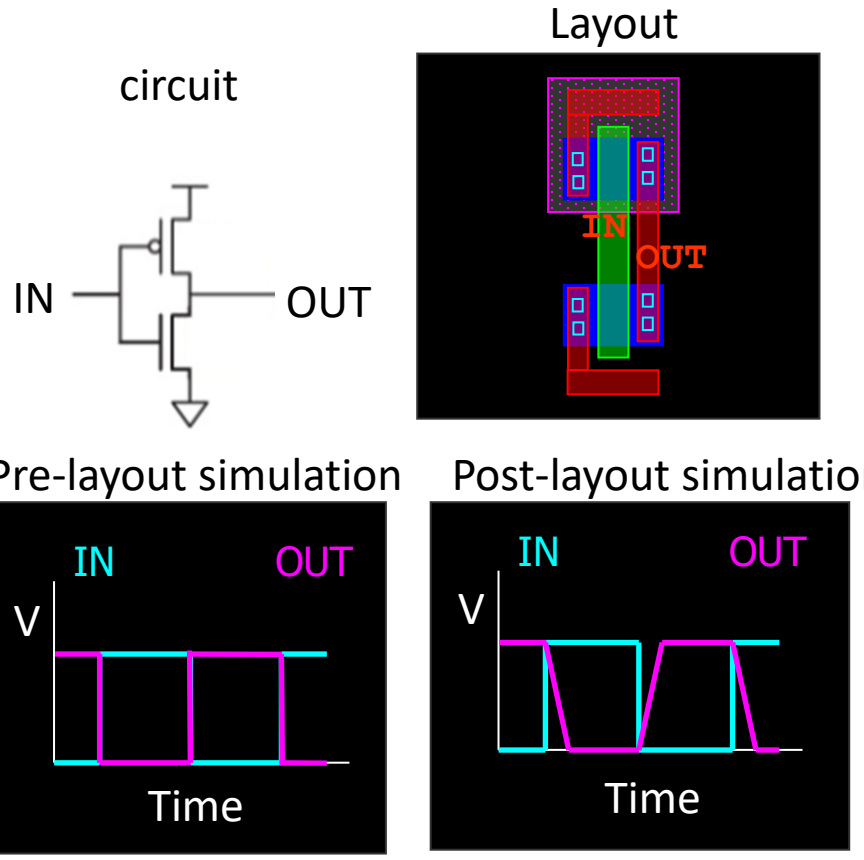
Parasitic extraction…why?

- In ICs, parasitic devices are the capacitors, resistors, and inductors that aren't included in the original circuit design but exist due to the non-ideal nature of the interconnect wires.

Parasitic capacitances in interconnects



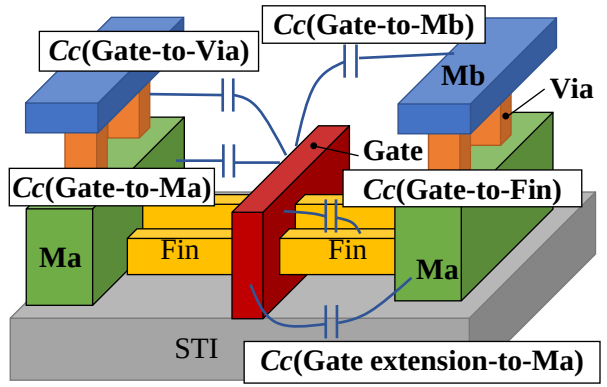
Source: Pucknell and Eshraghian(1998)

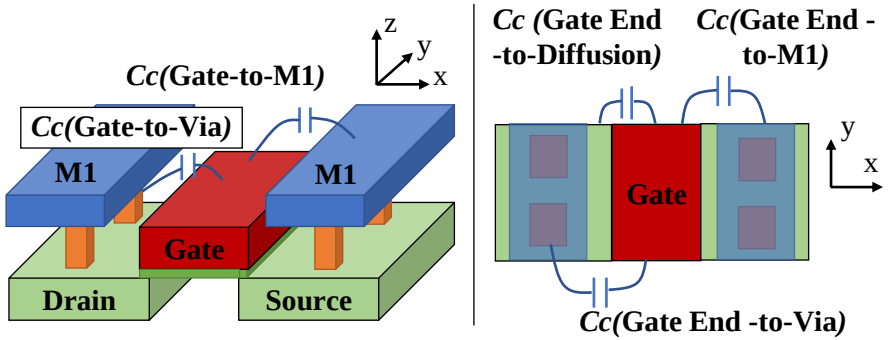


Middle End OF Line (MEOL)

- The middle end of line (MEOL) represents the interconnects around the device region. The MEOL parasitic capacitances are not part of the device models (e.g., BSIM).

- MEOL parasitic capacitances have a major impact on a device performance, especially in advanced process nodes (i.e., finfets).





Parasitic capacitance extraction methods

- The parasitic extraction has three main Methods:
  - **Numerical Methods (aka field-solvers):**

    Use Laplace formula to get the parasitic value by using (FEM, FDM, BEM,…).

    The most accurate but the worse performance.

  - **Analytical Methods:**

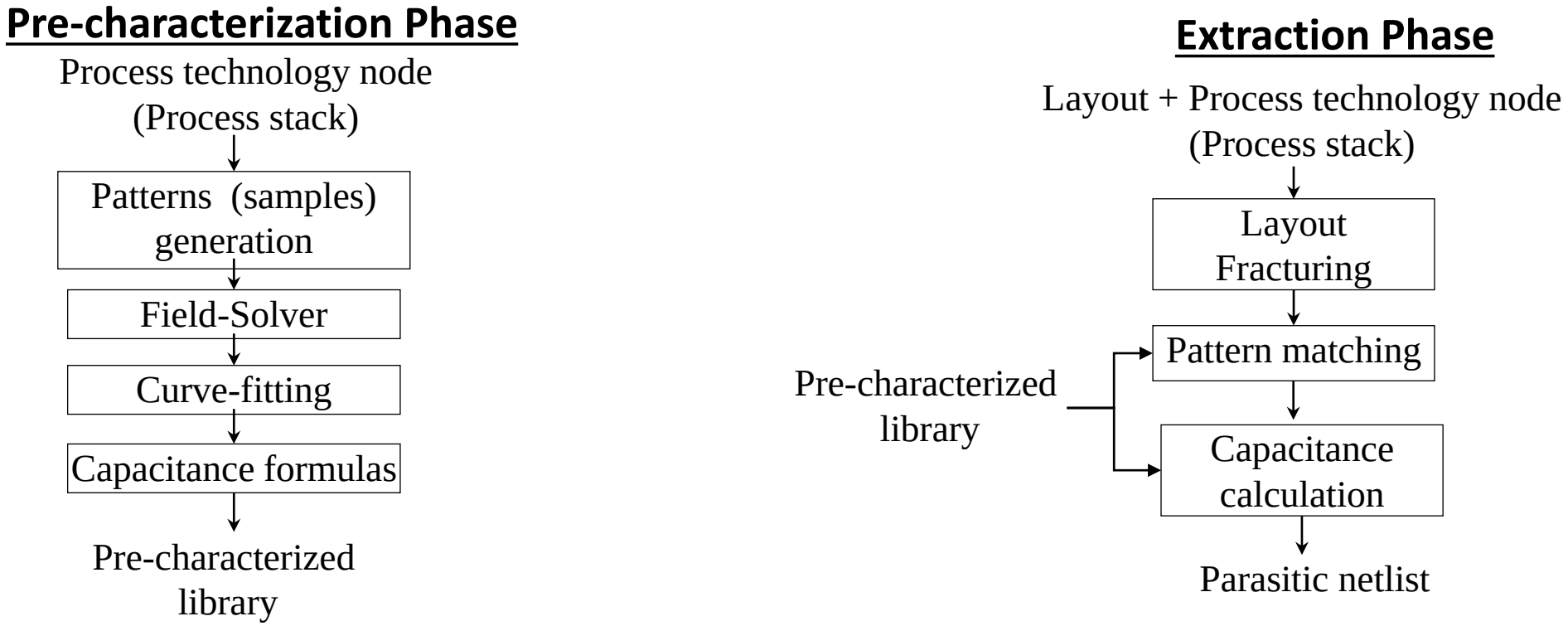
    Use physical formulas to calculate the parasitic effects.

  - **Empirical and semi-analytical Methods:**

    Use pattern matching, curve fitting and lookup tables. (commercial rule-based).

Rule-based capacitance extraction

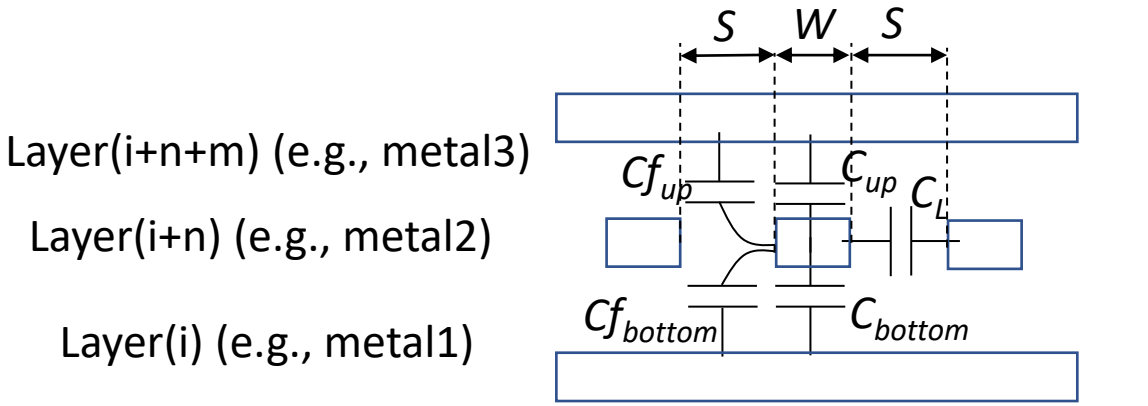
- The Extraction Flow is mainly divided into two main phases:
  - Calibration (pre-characterized library).
  - Layout parasitic extraction.



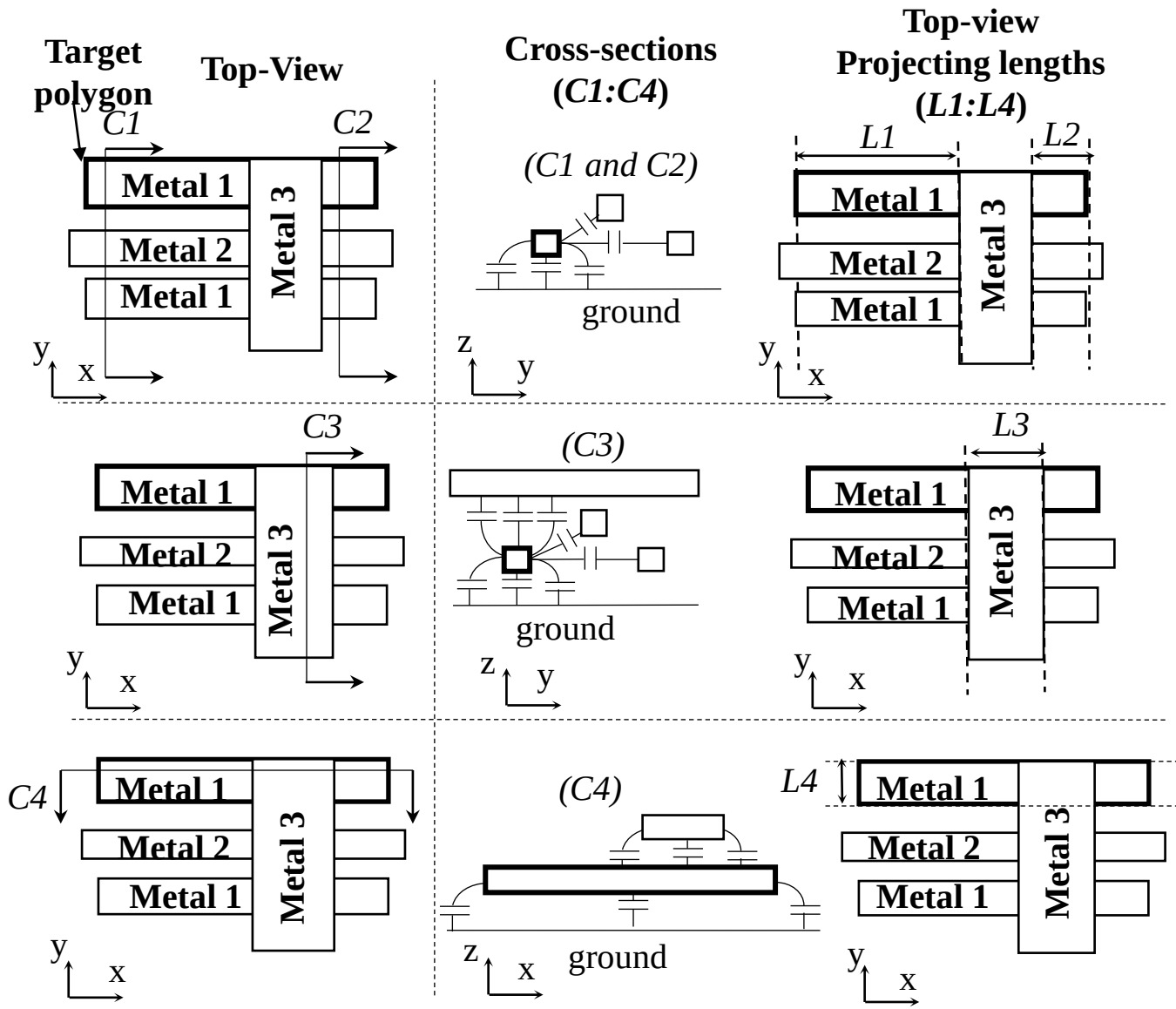
Rule-based capacitance extraction

- The 2.5D extraction aims to:

1. Fracture into cross-sections.
2. Pattern matching.
3. Capacitance calculations.

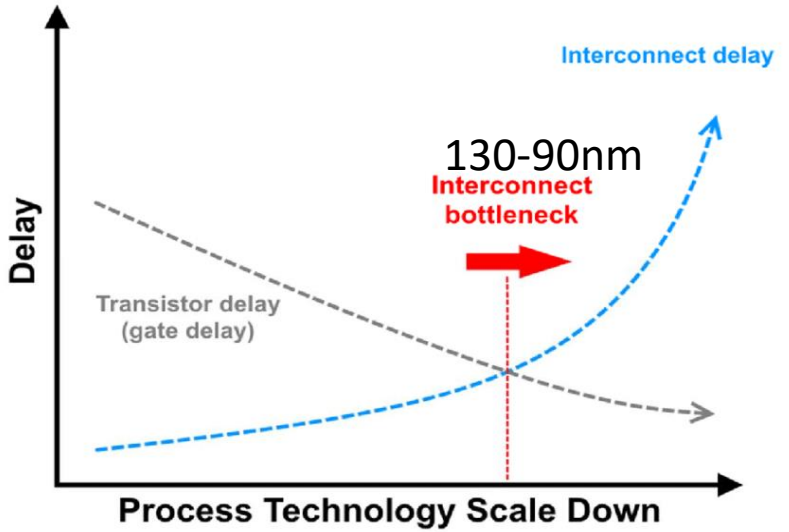


An Example of 2D-cross-section pattern with 5 different capacitance formulas



Problem definition

- In advanced process nodes, the interconnect parasitic effects dominate the overall circuit performance requiring more accurate parasitic models.



The impact of interconnect parasitic on overall circuit delay [1] and [2]

- The main problems of MEOL in rule-based extraction flows:
  - Pattern mismatches
  - Limited pattern coverage.

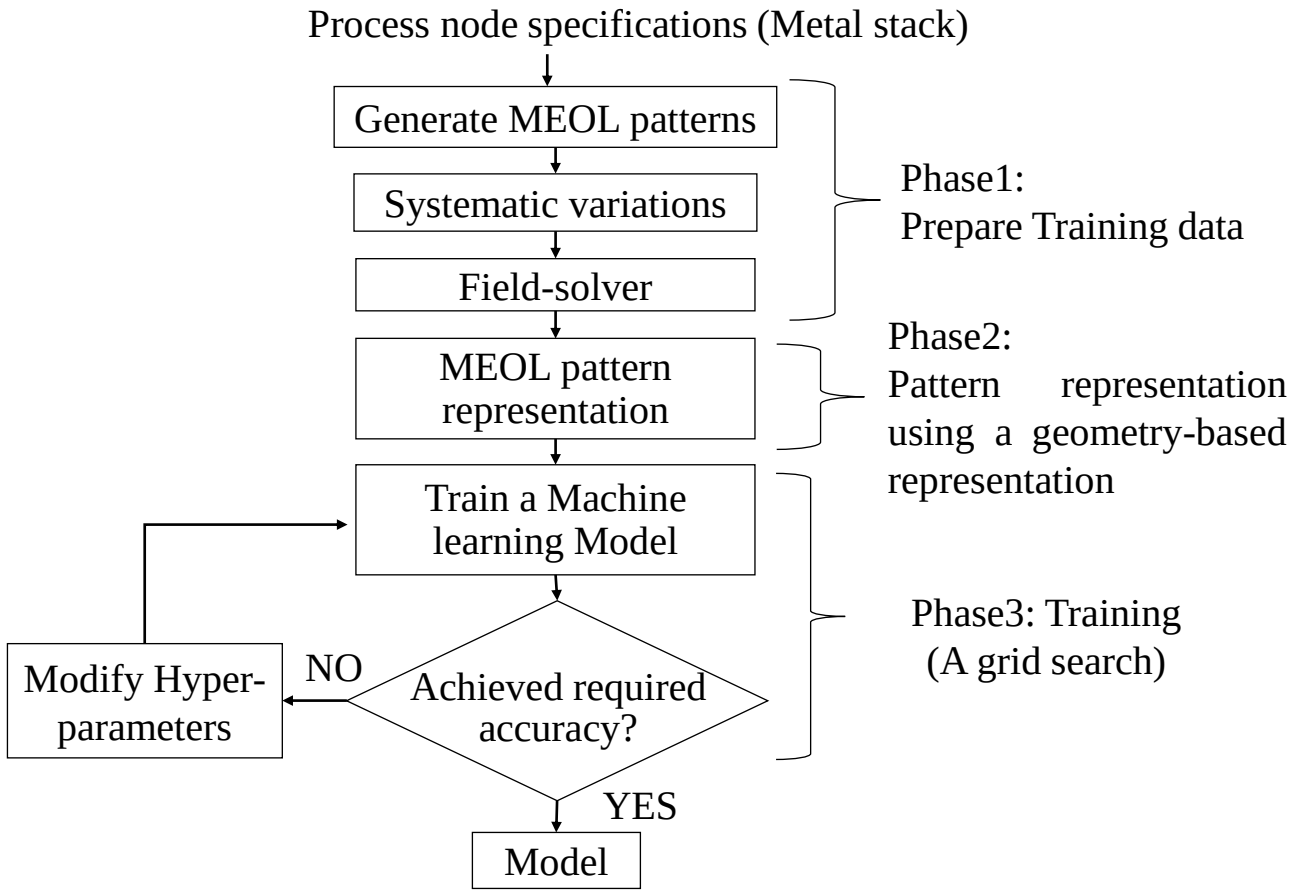
[1]A. Naeemi, C. Pan, A. Ceyhan, R. M. Iraei, V. Kumar, and S. Rakheja, "BEOL scaling limits and next generation technology prospects," in *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, Jun. 2014, pp. 1–6. doi: 10.1145/2593069.2596672
[2] G. Bell, "Growing challenges in nanometer timing analysis," *EE Times*, Oct. 18, 2004.

Machine Learning MEOL Compact Models

- Compact machine learning models that predict MEOL parasitic capacitances efficiently:
  - They predict different 3D fringing capacitances.
  - They mitigate pattern mismatches.
  - They have a high pattern coverage.
- Geometry-based pattern representation to represent MEOL layout patterns.
- Two machine learning methods are used and compared to each other:
  - Neural networks.
  - Support vector regressions.

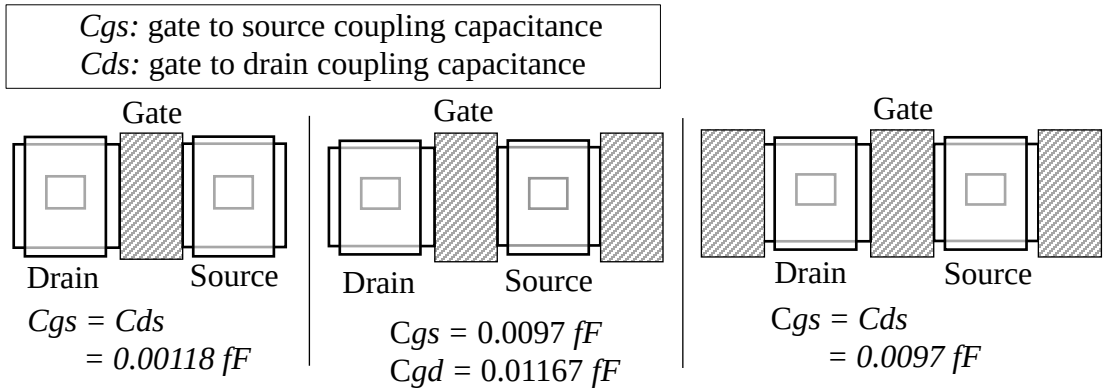
Machine Learning MEOL Compact Models

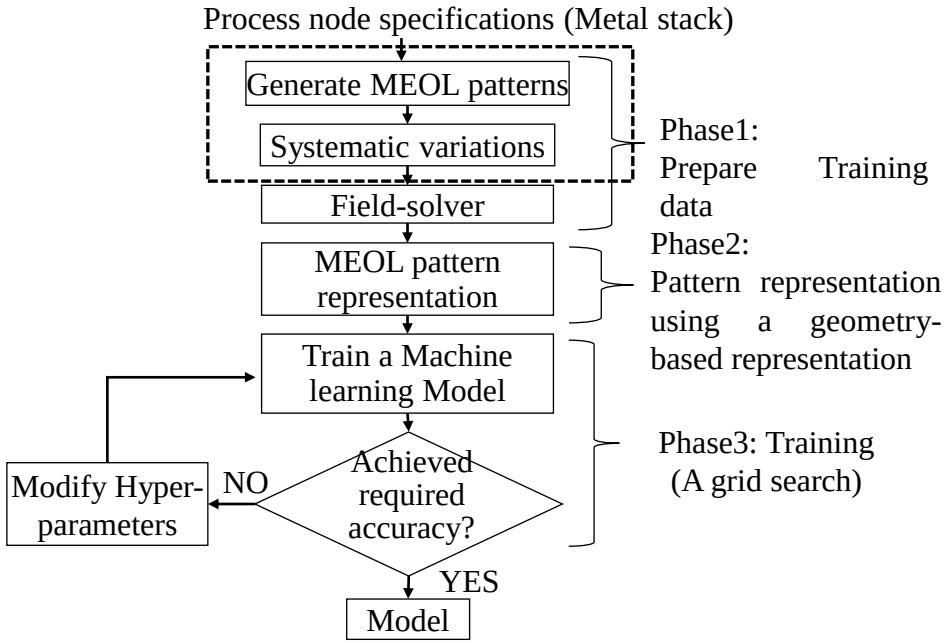
The implementation process of MEOL parasitic capacitance models is shown in this slide:



Machine learning MEOL models: Training patterns

- Training dataset: 25K MEOL patterns.
- Generation method:
  - Obtained from several real designs including DAC, cache memory,…
  - Random patterns from (1X to 10X) of minimum technological dimensions.
- Important Factors:
  - Multi-Finger devices.
  - Multi-Dielectric Stacks.





Machine learning MEOL models: Training patterns

- **Multi-dielectric Environment:**

  Problem:

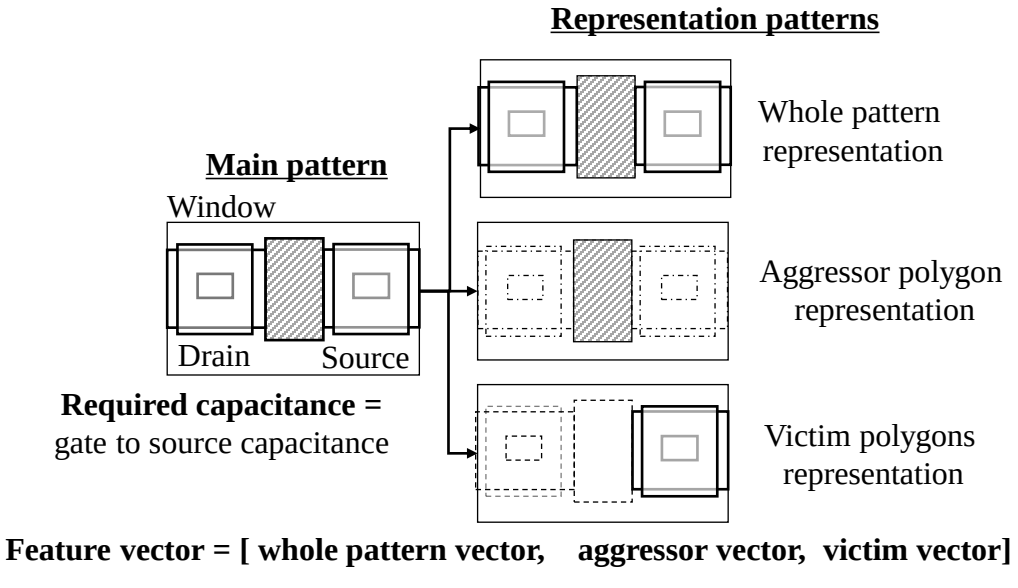
  - Each device and corresponding MEOL interconnects have specific surrounding dielectrics. Such dielectrics have different characteristics (e.g, dielectric constant, thickness, ….

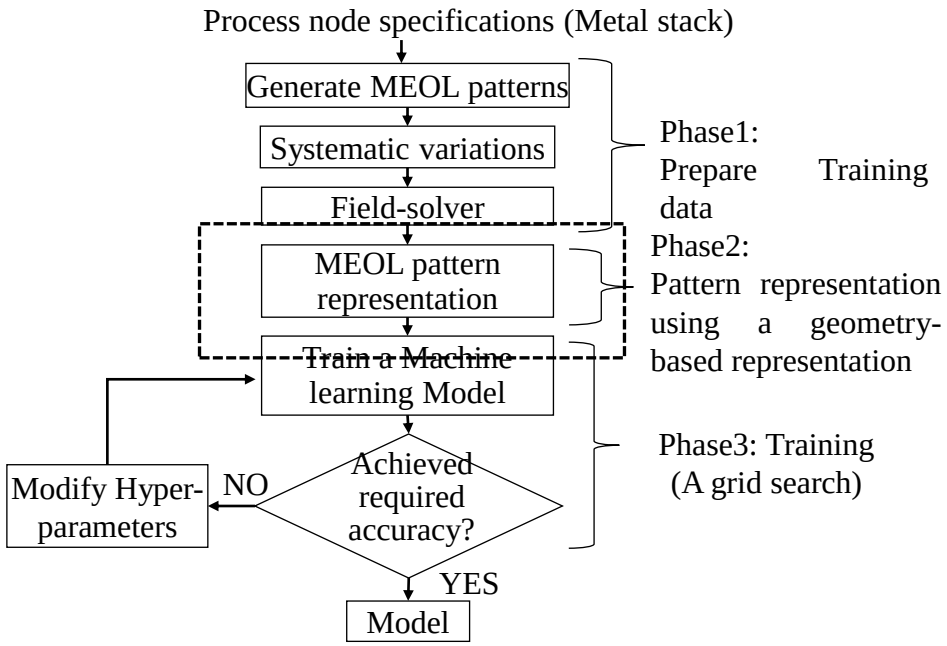
  Solution:

  - Each process technology must have its own models.
  - Each device type must have its own models.
  - In other words, there is a model per device per process technology node.

Machine learning MEOL models: Feature Extraction

- The inputs of parasitic capacitance machine learning models should introduce:
  - Geomatical information of the 2D cross-section pattern.
  - Aggressor polygons.
  - Victim polygons.



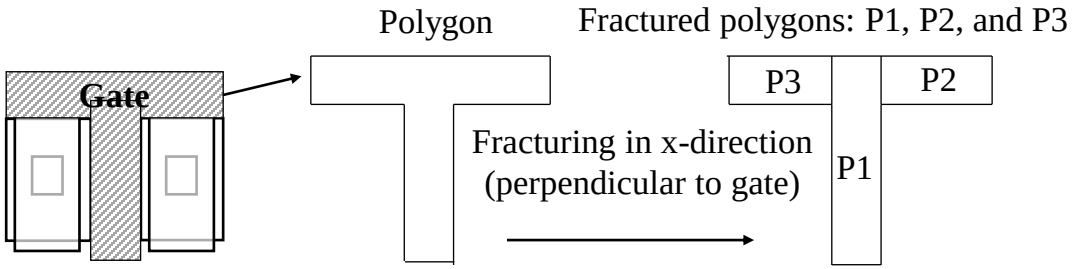


Machine learning MEOL models: Feature Extraction (Steps)

- Fracture MEOL polygons.
- Create a feature vector for each MEOL layer.
- Create a feature vector for Vias and Fins.
- Merge the vectors and create a final input feature vector.

Machine learning MEOL models: Feature Extraction (Fracture polygons)

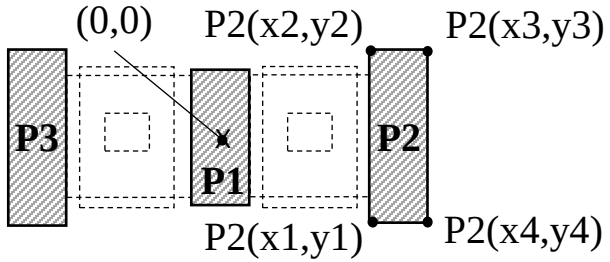
- The purpose is to fracture the polygons into quadrilateral shapes.
- The fracturing is done in x-direction (perpendicular to gate), then in y-direction (parallel to gate).



Vector = [layer1; layer2; layer3; …] polygons

Machine learning MEOL models: Feature Extraction (Feature Vector)

- Each MEOL layer is represented by its vertices.



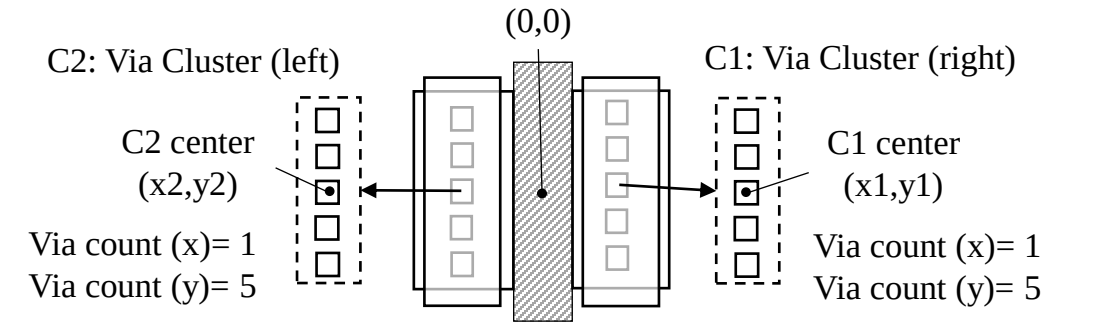
Gate/poly feature Vector =

[x1, y1, x2, y2, x3, y3, x4, y4 For P1: Center polygon
, x1, y1, x2, y2, x3, y3, x4, y4 For P2: 1st right polygon
, x1, y1, x2, y2, x3, y3, x4, y4] For P3: 1st left polygon

Vector (layer) = [center, 1st right, 1st left, 2nd right, 2nd left, …] polygons

Machine learning MEOL models: Feature Extraction (Feature Vector for Vias and Fins)

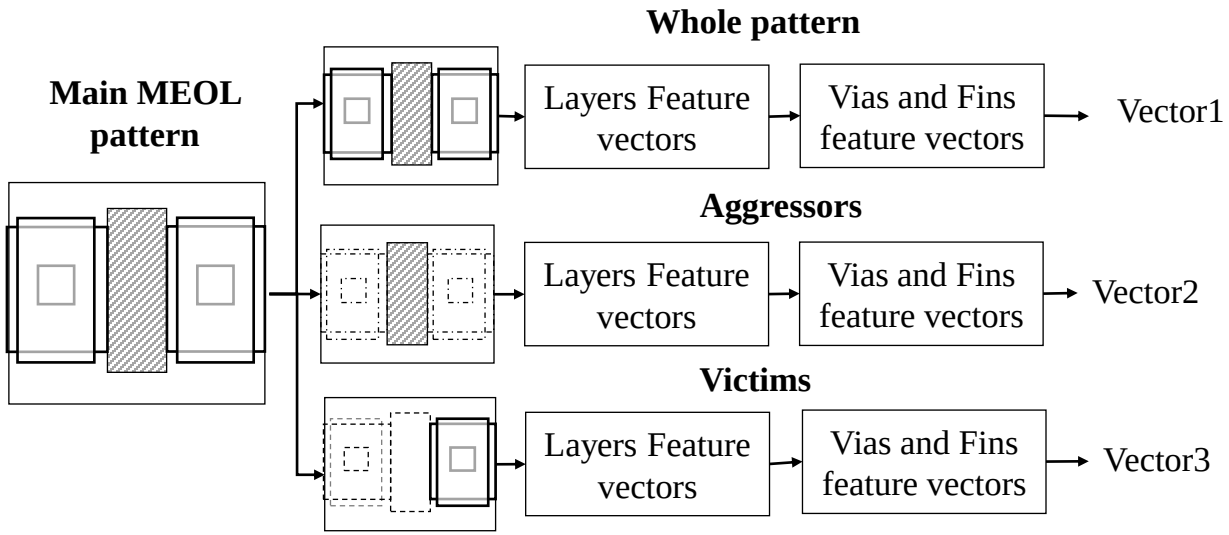
- The vias are represented by clusters.



Via feature vector =
[x1,y1, via count(x), via count (y), via width, via spacing For C1
, x2,y2, via count(x), via count (y), via width, via spacing] For C2

- The fins are represented by fin width and fin spacing.

Machine learning MEOL models: Feature Extraction (Input Feature Vector)



Final input feature vector = [Vector1, Vector2, Vector3]

Vector1/2/3 = [layer1; layer2; layer3; vias; fins] geometries

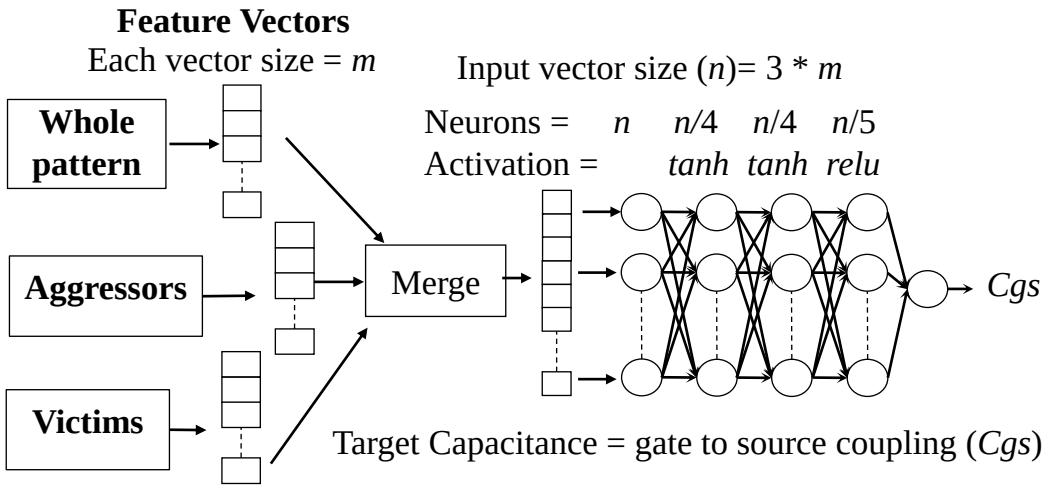
Vector (layer) = [center; 1st right; 1st left; 2nd right; 2nd left; …] polygons (vertices)

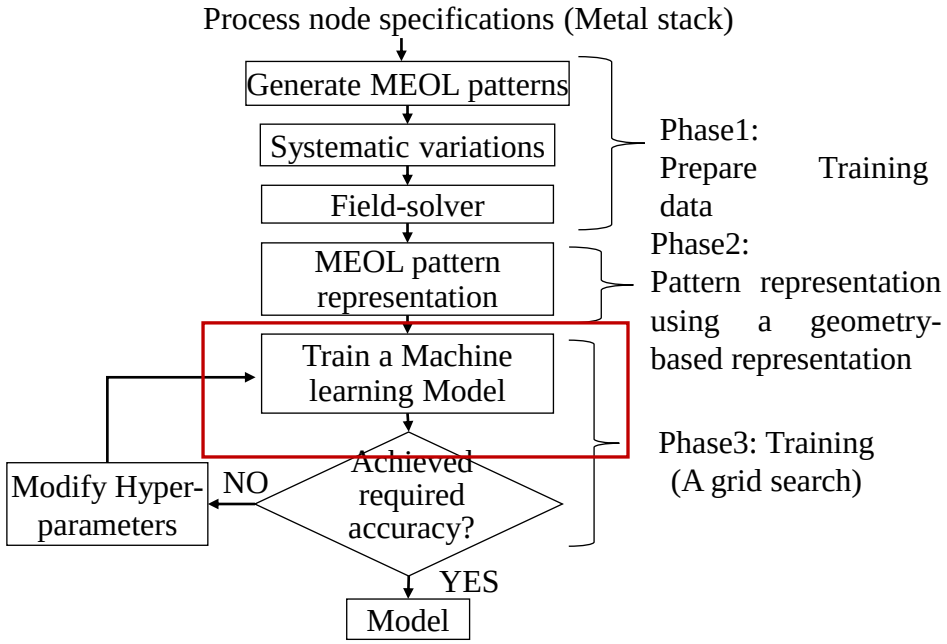
Vector (via) = [cluster center; via count (x-direction); via count (y-direction); width; spacing]
Vector (fin) = [fin width; fin spacing]

Machine learning MEOL models: Model's Creation (Neural networks)

•Training Hyper Parameters of MEOL Parasitic Capacitances NN Models.

Parameter	Value
Training set	80% (20K patterns)
Test set	20% (5K patterns)
Batch size	500
Validation set	10% (2K patterns)
Loss function	Mean square error
Learning rate	1e-3
Batch normalization	YES
Epochs	500
Optimizer	Adam





Machine learning MEOL models: Model's Creation (Neural networks)

Training on: Intel Xeon(R) E5- 2680, 2.50GHz with 8 CPUs and 16G of RAM

	28nm (MOSFET)	7nm (FINFET)
Input vector size (n)	696	681
Architecture	Three hidden layers (174, 174, 140 neurons, respectively)	Three hidden layers (170, 170, 136 neurons, respectively)
Training accuracy (MSE)	3.7e-3	4.3e-3
Test accuracy (MSE)	5.2e-3	5.8e-3
Training Time	3.6 hours for two models (1.8 hours per model)	13.8 hours for 6 models (2.3 hours per model)
Comment	MOS transistors may contain a lot of irregular structures, such as T shaped, I shaped, M1 over gate. However, it contains a smaller number of capacitance components.	FinFET structures are usually regular. However, They contain more 3D fringine parasitic capacitance components.

Machine learning MEOL models: Model's Creation (Support vector regression)

	28nm	7nm
Kernel	Kernel: radial basis function (RBF)	Kernel: radial basis function (RBF)
Regularization (C)	8	8
Epsilon	0.1	0.1
Gamma	0.3	0.3
Training accuracy (MSE)	4.1e-3	5.7e-3
Test accuracy (MSE)	6.7e-3	7.1e-3
Training Time	1.7 hours for two models (0.85 hours per model)	6.18 hours for 6 models (1.03 hours per model)

Intel Xeon(R) E5- 2680, 2.50GHz with 8 CPUs and 16G of RAM

Experimental results: Test coverage

	28nm	7nm
Test coverage	~15M devices (RO, VCO, and DAC)	~20M devices (RO, SRAM, and PLL clock generator)
Runtime (per pattern)	NN: 2.43ms SVR: 2.18ms Rule-based: 2.52ms Field-solver 3D: 240ms	NN: 2.61ms SVR: 2.4ms Hybrid: 235ms Field-solver 3D: 264ms

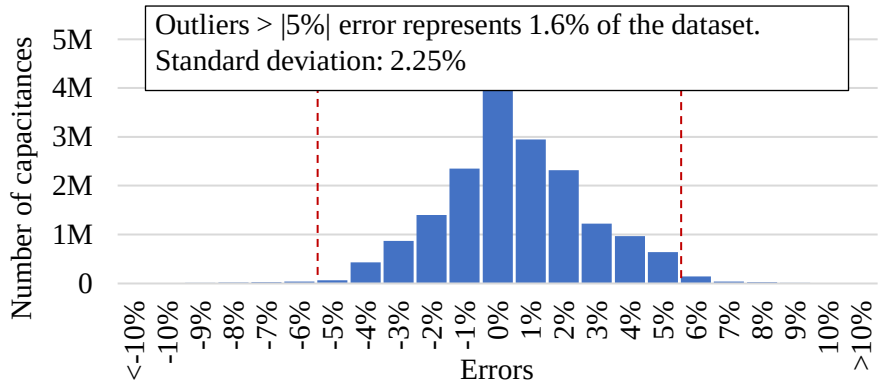
Intel Xeon(R) E5-2680, 2.50GHz, 1 CPU, and 16G of RAM

- Comparison is relative to 3D field-solver
- In 28nm, the comparison covered three methods: the proposed NN models , SVR models, and a rule-based tool.
- In 7nm, the comparison covered three methods: the proposed NN models , SVR models, and a Hybrid tool.

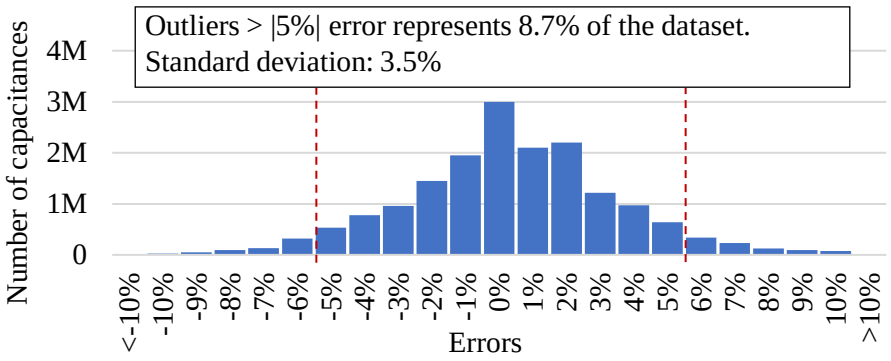
The hybrid tool uses rule-based engine to extract interconnects, whereas it uses a field-solver to extract MEOL.

Relative errors (28nm)

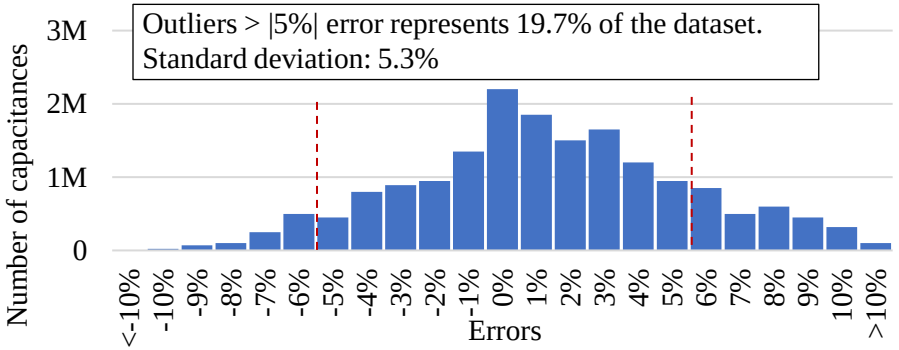
NN



SVR



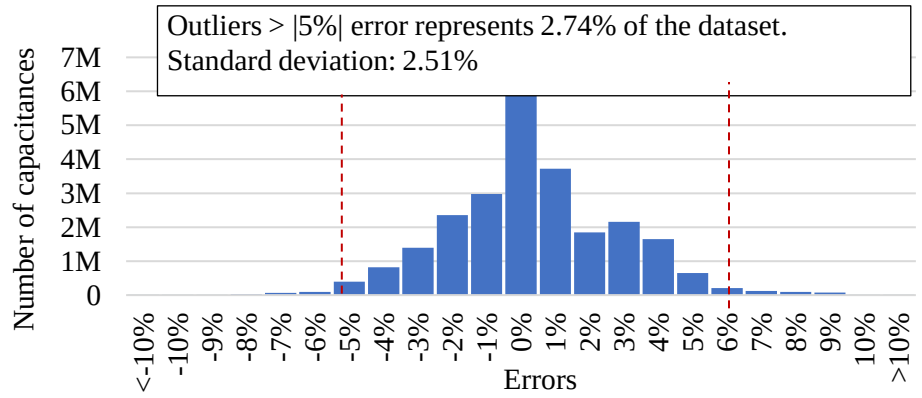
Commercial Rule-based



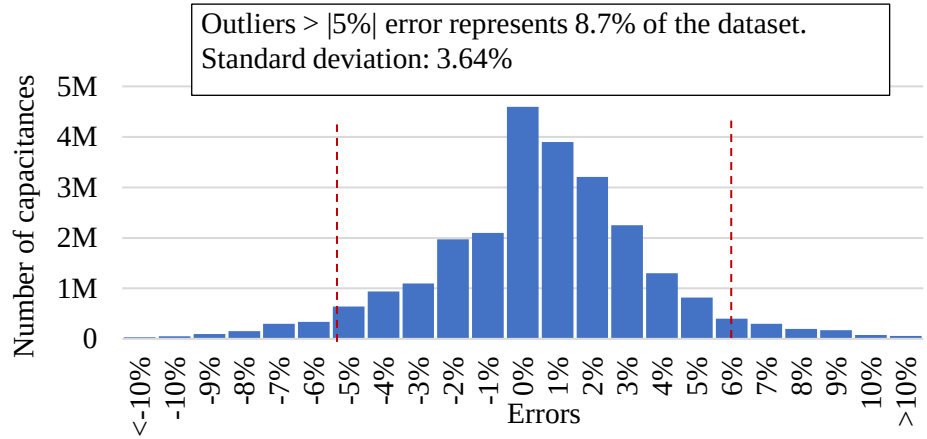
28nm	SVR	NN	Rule-based
Mean of relative errors	0.401%	0.12%	1.03%
Standard deviation	3.5%	2.25%	5.3%
Outliers > 5%	8.7%	1.6%	19.7%

Relative errors (7nm)

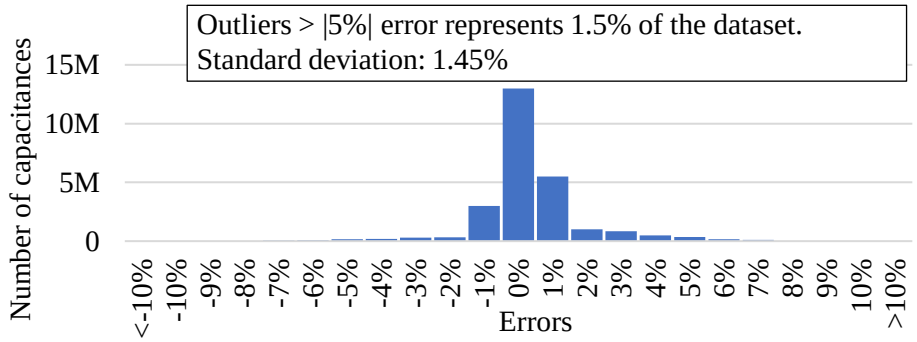
NN



SVR



Commercial Hybrid tool



7nm	SVR	NN	Hybrid
Mean of relative errors	0.51%	0.093%	0.017%
Standard deviation	3.64%	2.51%	1.45%
Outliers > 5%	8.9%	1.74%	1.5%

Summary

- The MEOL parasitic capacitance extraction using rule-based methods suffers from:
  - Pattern mismatches.
  - Pattern coverage.
- Set of machine learning compact models are implemented to:
  - Extract MEOL parasitic capacitances efficiently.
  - Reduce pattern mismatches with MEOL extraction.
  - Improve pattern coverage in MEOL extraction.
- A novel geometry-based pattern representation is proposed to represent MEOL patterns.
- Experimental results show significant accuracy and runtime improvements.
  - The models were tested on more than 35M devices of 28nm and 7nm process technology nodes.
  - More than 95% of the extracted capacitances have relative errors < 5%
  - They are ~100X faster than field solvers and hybrid tools.

Thanks