Lamina: Low Overhead Wear Leveling for NVM with Bounded Tail

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Non-Volatile Memory is Trending

- Commodity NVM is known for its high capacity, low energy consumption, and byte addressing ability.
- Using NVM as a large alternative memory device for DRAM
- Commercial non-volatile memory was available

(Intel Optane DC)

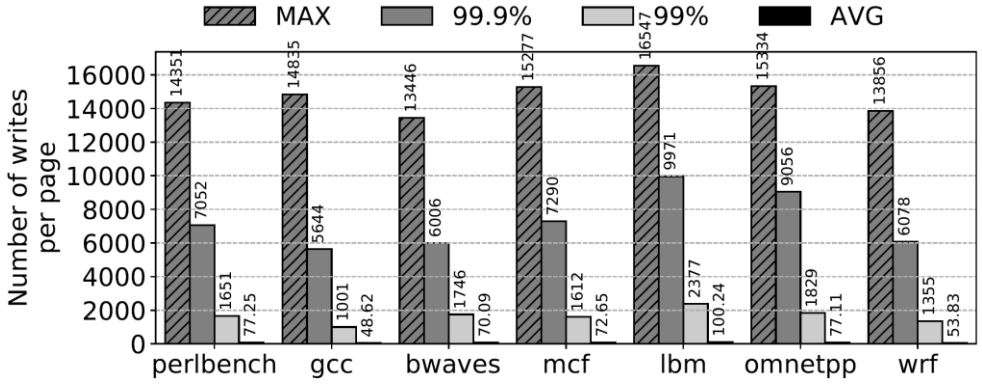
Lifetime Defect

- **Lifetime is short**

Memory Technology	Read Latency (ns)	Write Latency (ns)	Write Endurance (Times)
Flash SSD	25 000	200 000	10^5
DRAM	80	80	$>10^{16}$
PCM	50–80	150–1 000	10^8
STT-RAM	6	13	10^{15}
ReRAM	10	50	10^{11}
Intel Optane DCPMM	169 (sequential), 305 (random)	90	10^8

Haikun Liu and Di Chen and Hai Jin and Xiaofei Liao and Binsheng He and Kan Hu and Yu Zhang (2021). A Survey of Non-Volatile Main Memory Technologies: State-of-the-Arts, Practices, and Future Directions. *J. Comput. Sci. Technol., 36(1), 4–32.*

- **Skew writes**



Wear Leveling

- **Age-based methods**
  - Segment Swapping (ISCA 09)

  Recording the write count of each segment. If a segment is written too many times, this segment is swapped with the least used segment with the help of an address mapping table

- **Randomization-based methods**
  - Random Shuffle (Security refresh [ISCA 10], Kevlar [FAST 19])

  Achieving the uniform distribution of write accesses

  - Start-Gap (MICRO 09, MSST 20)

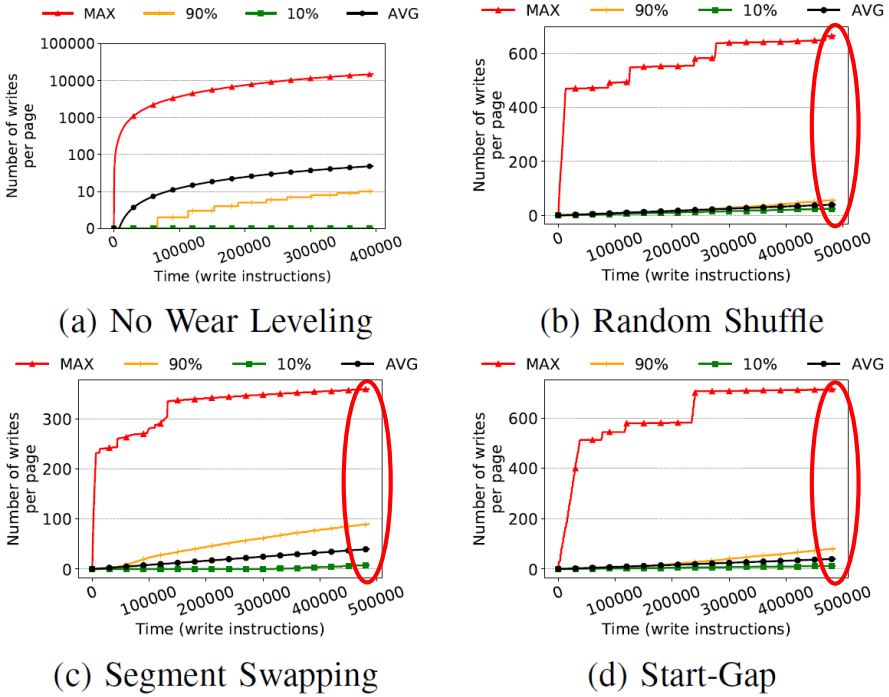
  Using two registers (start register and gap register) to swap the selected memory area with its adjacent area

Outline

- Introduction
- **Tail Wear and Accuracy Observations**
- Lamina Design
- Evaluation

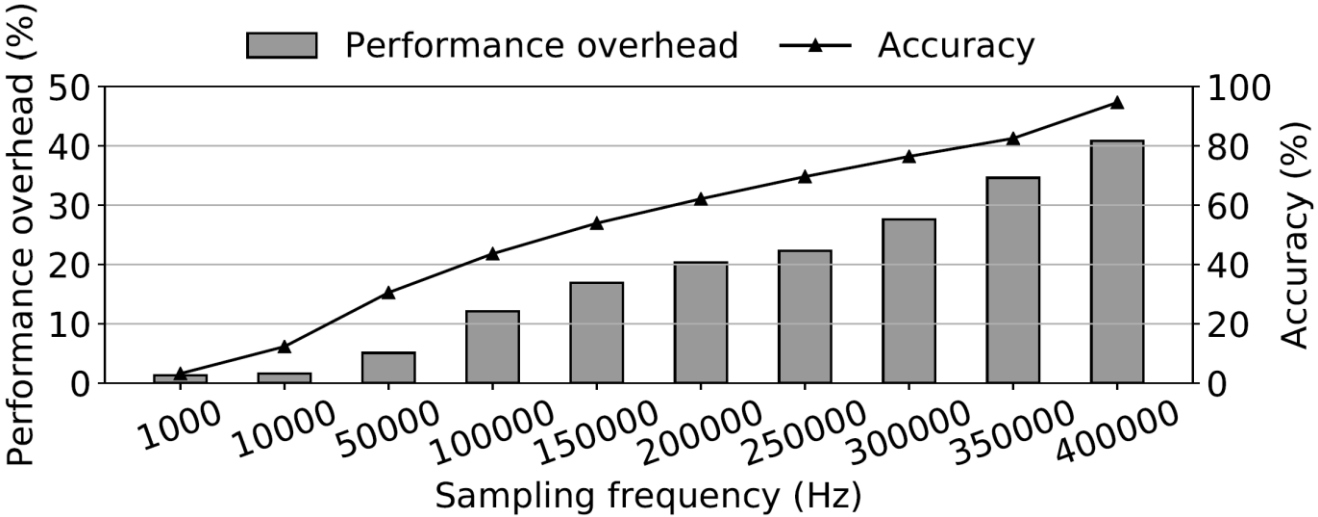
Tail Wear Problem

- Unbounded tail wear is the root cause that makes the actual wear leveling result deviate from the ideal result



Dilemma between Performance and Accuracy

- High frequency sampling will greatly degrade the performance
- Trade-off between accuracy and performance



- Previous work: Kevlar [FAST 19], Thermostat [ASPLOS 17]

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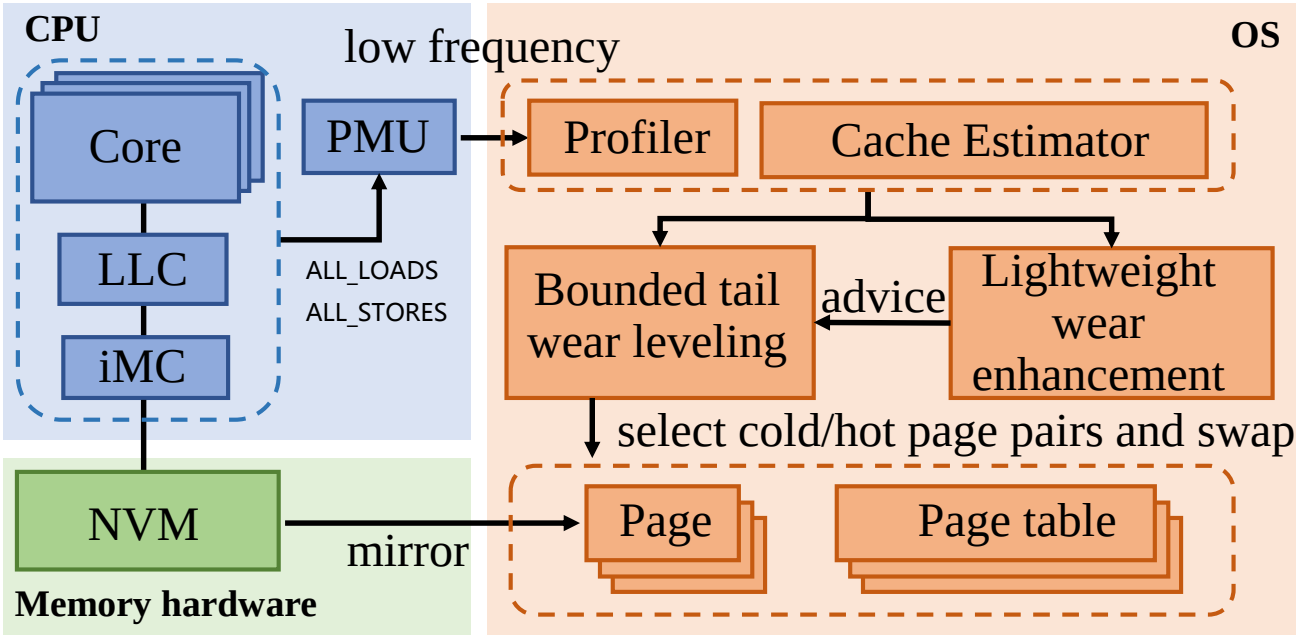
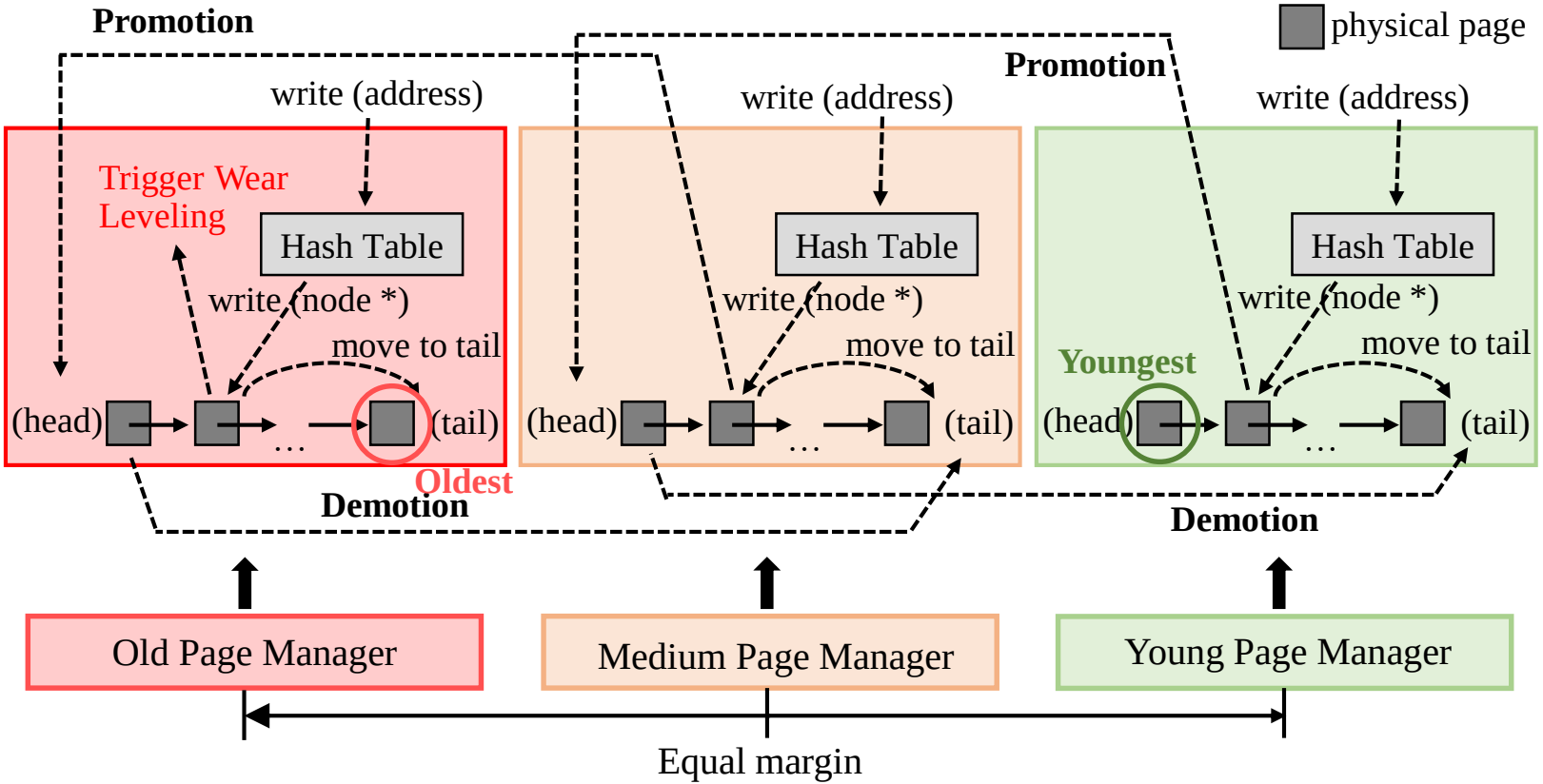
Lamina Overview

- Lamina is implemented at the OS level



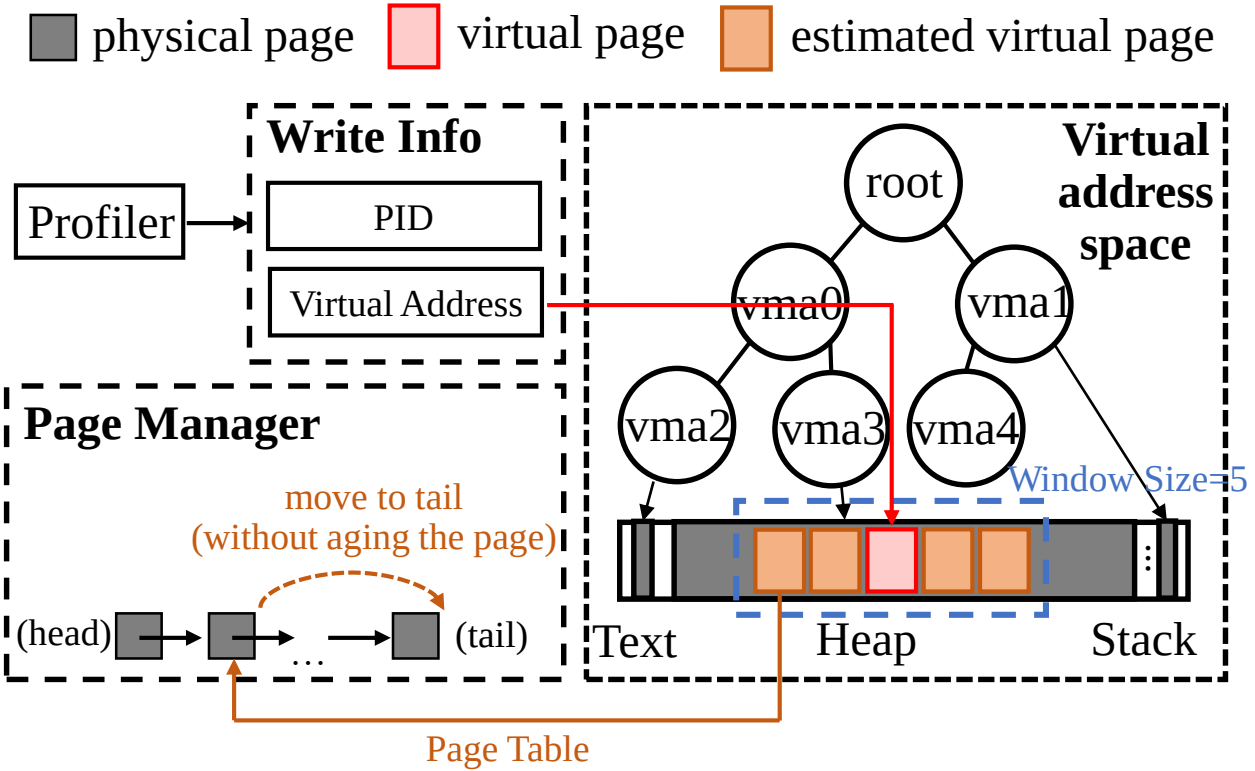
Bounded Tail Wear Leveling (BTWL)

- BTWL discriminates the pages into different ages and manage them



Lightweight Wear Enhancement (LWE)

- LWE estimates the write operations lost during sampling

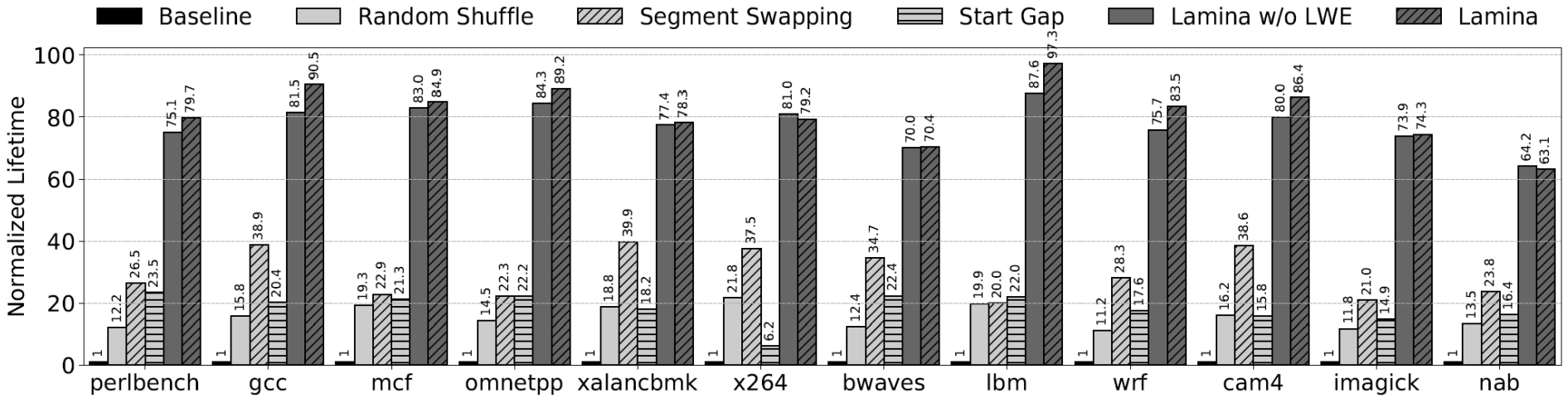


Evaluation Overview

- **Baseline**
  - Random Shuffle (ISCA 10, FAST 19)
  - Segment Swapping (ISCA 09)
  - Start-Gap (MICRO 09, MSST 20)
- **Experimental Setup**
  - Intel Core i7-8750H processor
  - 32 GB DDR4 memory
  - Linux kernel version 5.4.25
- **Benchmark**
  - SPEC CPU 2017

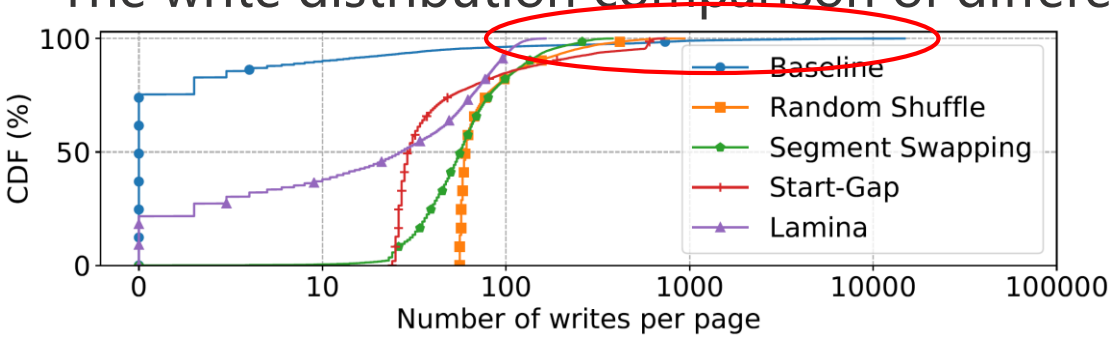
Lifetime Improvement

- Compared to the baseline, Lamina can increase the lifetime of NVM 81.4 times on average
- Compared with other wear leveling methods, Lamina can improve the lifetime of NVM significantly
- LWE to enhance the sampling data can improve the effect of Lamina

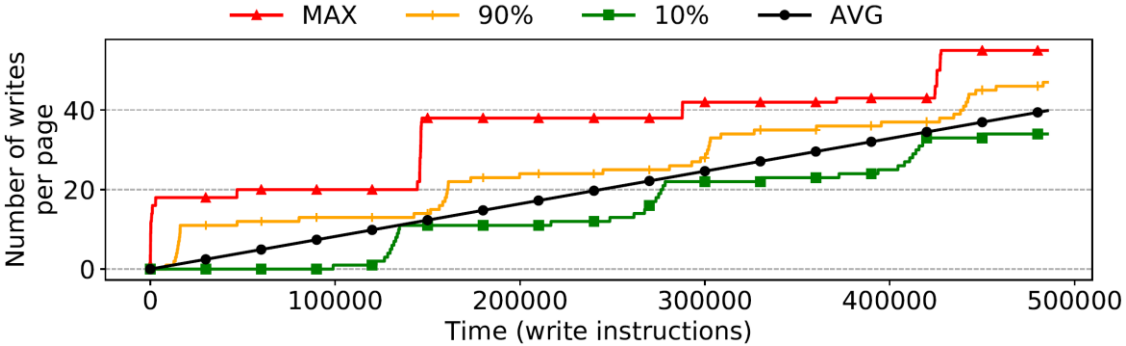


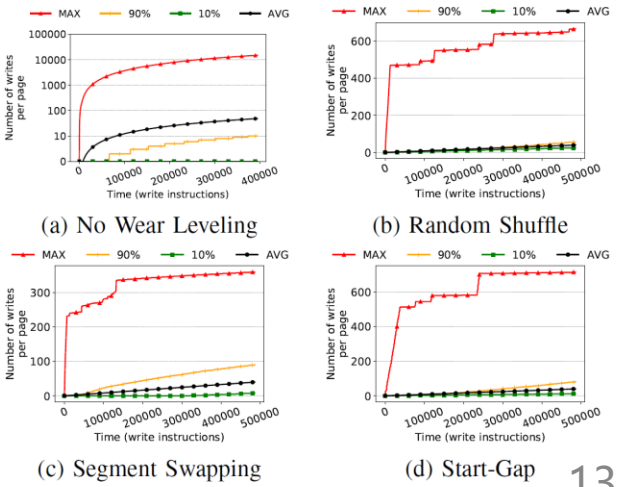
Analysis of Bounded Tail Wear Leveling

- The write distribution comparison of different wear leveling methods



- Lamina keeps approaching the average number of writes of all pages and limits the maximum number of writes

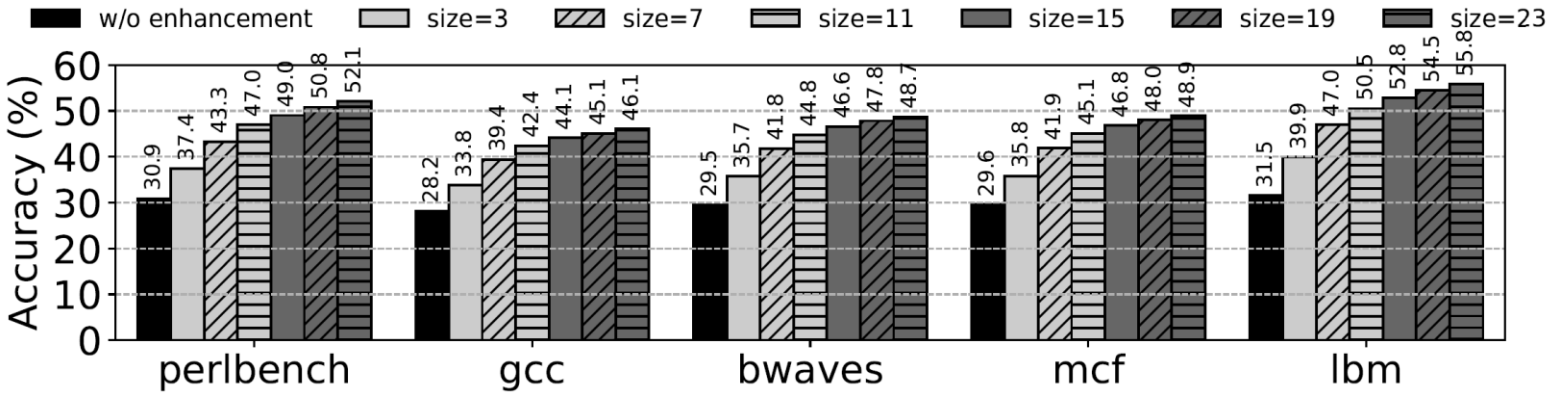




Analysis of Lightweight Wear Enhancement

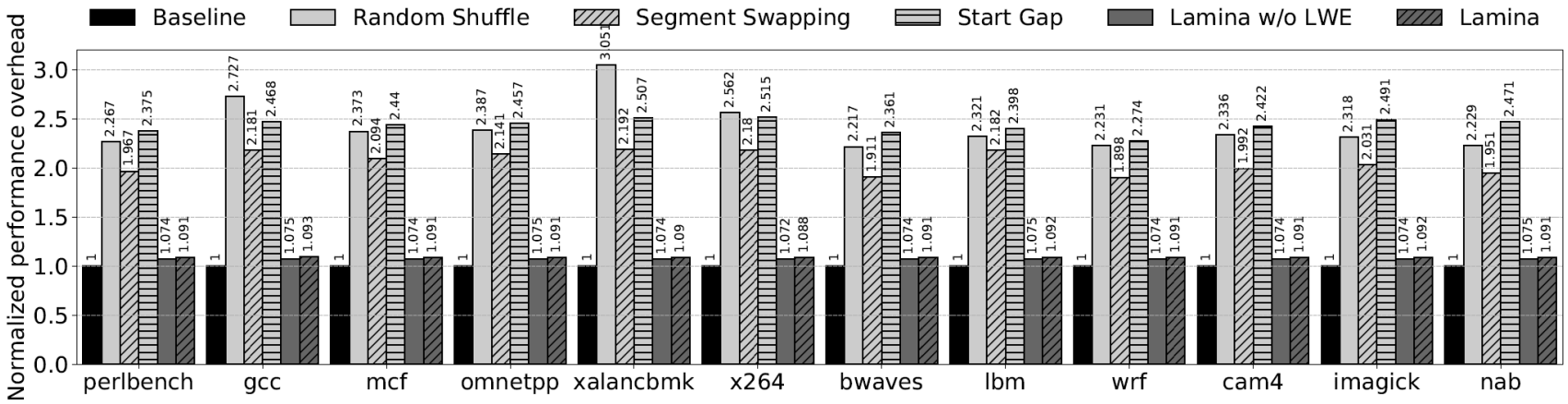
- The accuracy of the write operations and the improved accuracy of LWE under different window size

- If the window size is too large, the accuracy will converge



Overhead Discussion

- The performance overhead of Lamina is very small
- Lamina finds the most suitable pages for wear leveling and uses a low overhead sampling method
- Compared with the comparative wear leveling methods, Lamina only introduces a small number of write overheads caused due to page swapping



Takeaways

- **Problem**

  A very small percentage of extreme deviation significantly hurts the lifetime of NVM (Tail wear)

- **Solution (Lamina)**

  1. Bounded tail wear leveling
  2. Lightweight wear enhancement

- **Results**

  Lamina can significantly improve the lifetime of NVM with low overhead

Thank You !

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