Machine Learning for Electronic Design Automation

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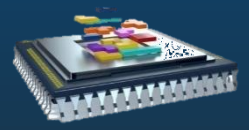
EDA **Enables** AI/ML Designs



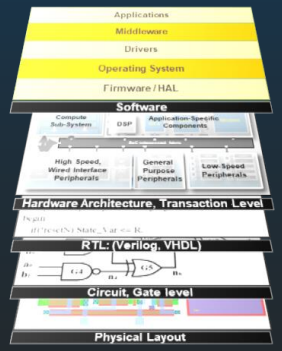
IP and Subsystems

IP Selection

"Reuse the right building blocks"

DSPs, Interfaces, Analog

Verification



Implementation

HW/SW Verification

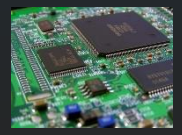
"Is it functionally correct?"

Hardware/Software, Power, Architecture, Safety, Security

Chip Implementation

"Optimized, advanced-node implementation"

Performance, Power, Cost



Board and Package

Packaging
PCB Integration

"Silicon into packages and parts into PCBs and 3D-IC heterogeneous integration"

Systems

System Analysis

"Does it work when put together?"

Electromagnetic, Thermal, Low Power, Computational Fluid Dynamics

Optimized flows to **enable AI/ML** chips and systems (for users)

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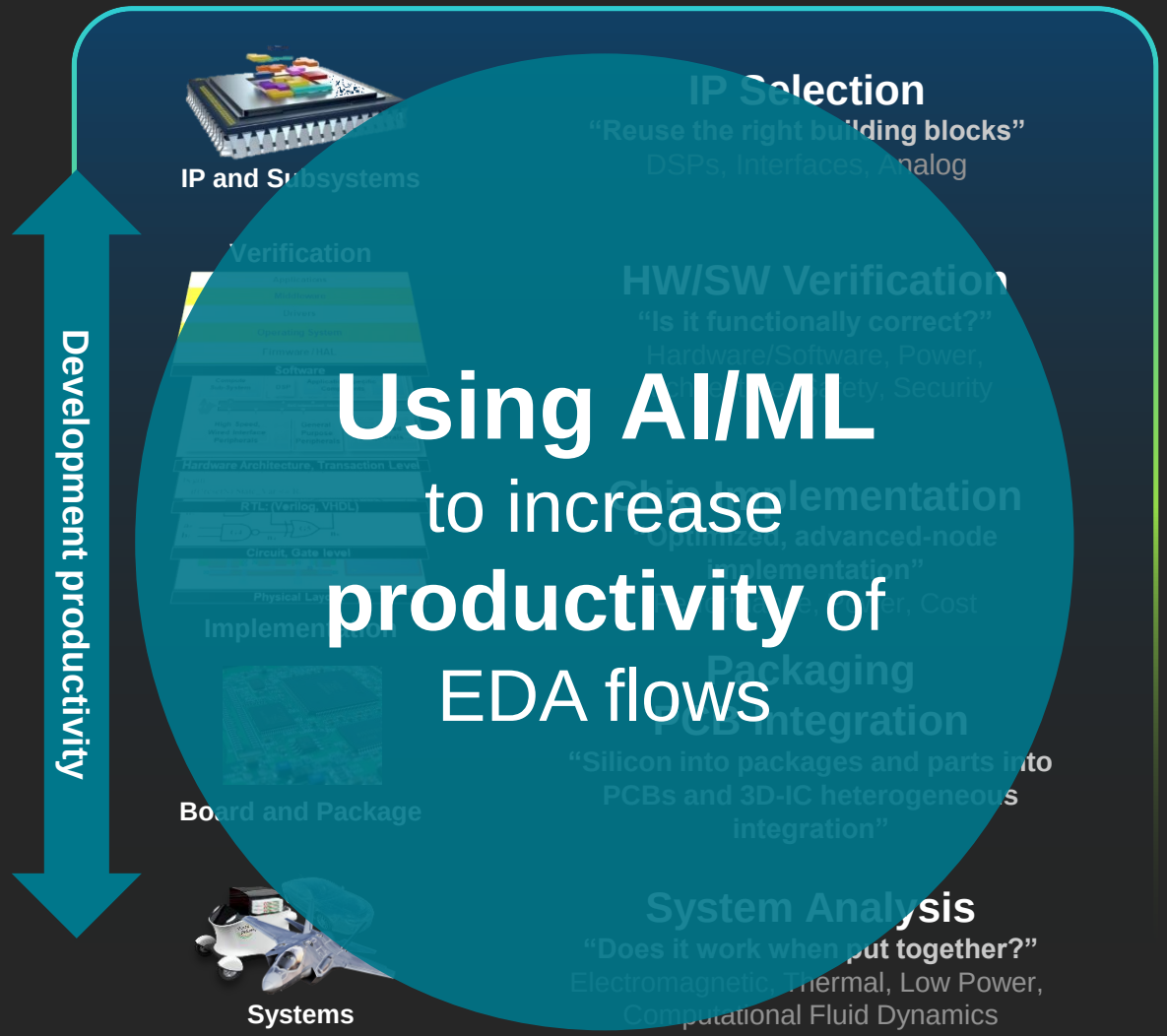
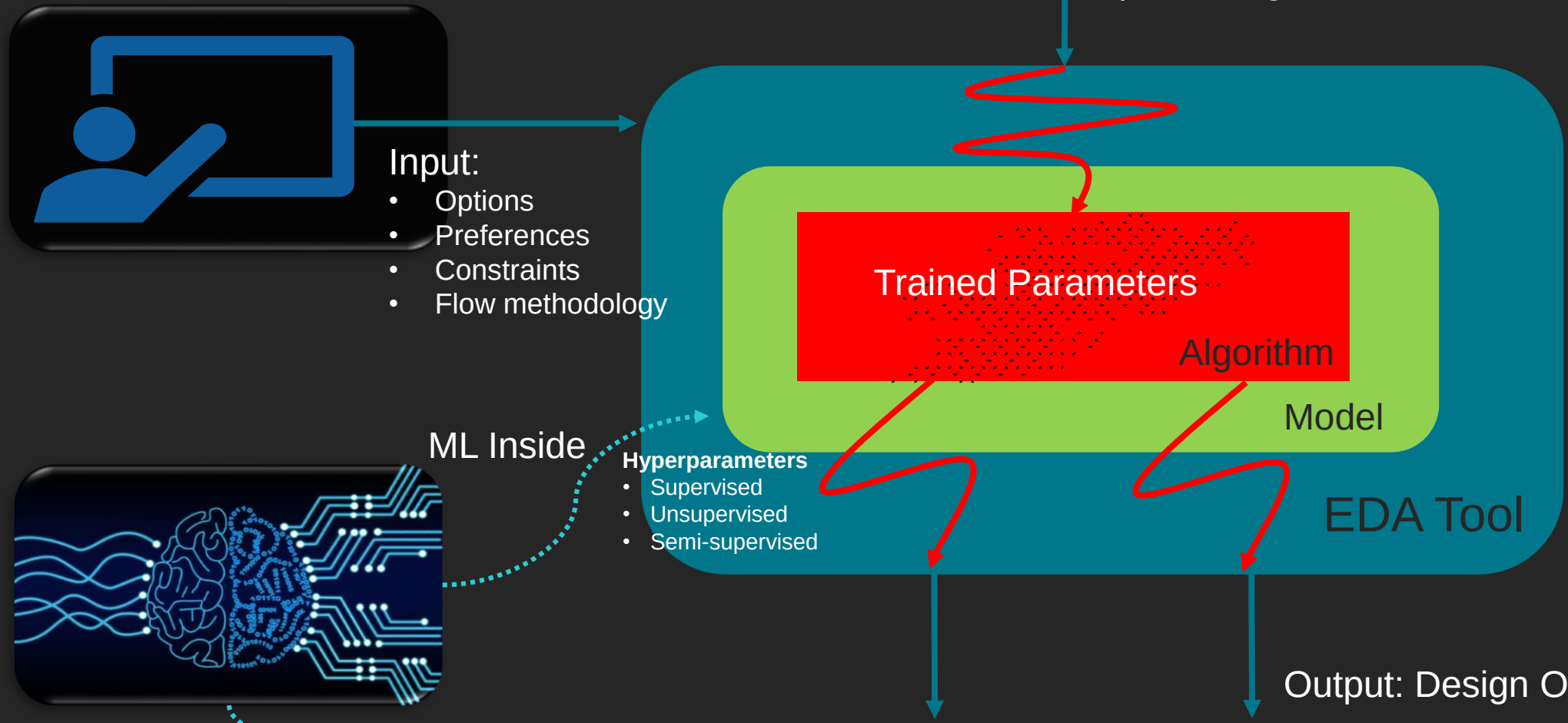
AI/ML is **Enabling EDA** too!



Optimized **flows** to **enable AI/ML** chips and systems

ML in Electronic Design Automation



ML Inside: Enhanced Delay Prediction

Training Data Extraction

Initial Design

Training

Model

Prediction Accuracy

Actual

Machine Learning Training

"Learns" to predict actual results from model inputs

Innovus™

ML Model

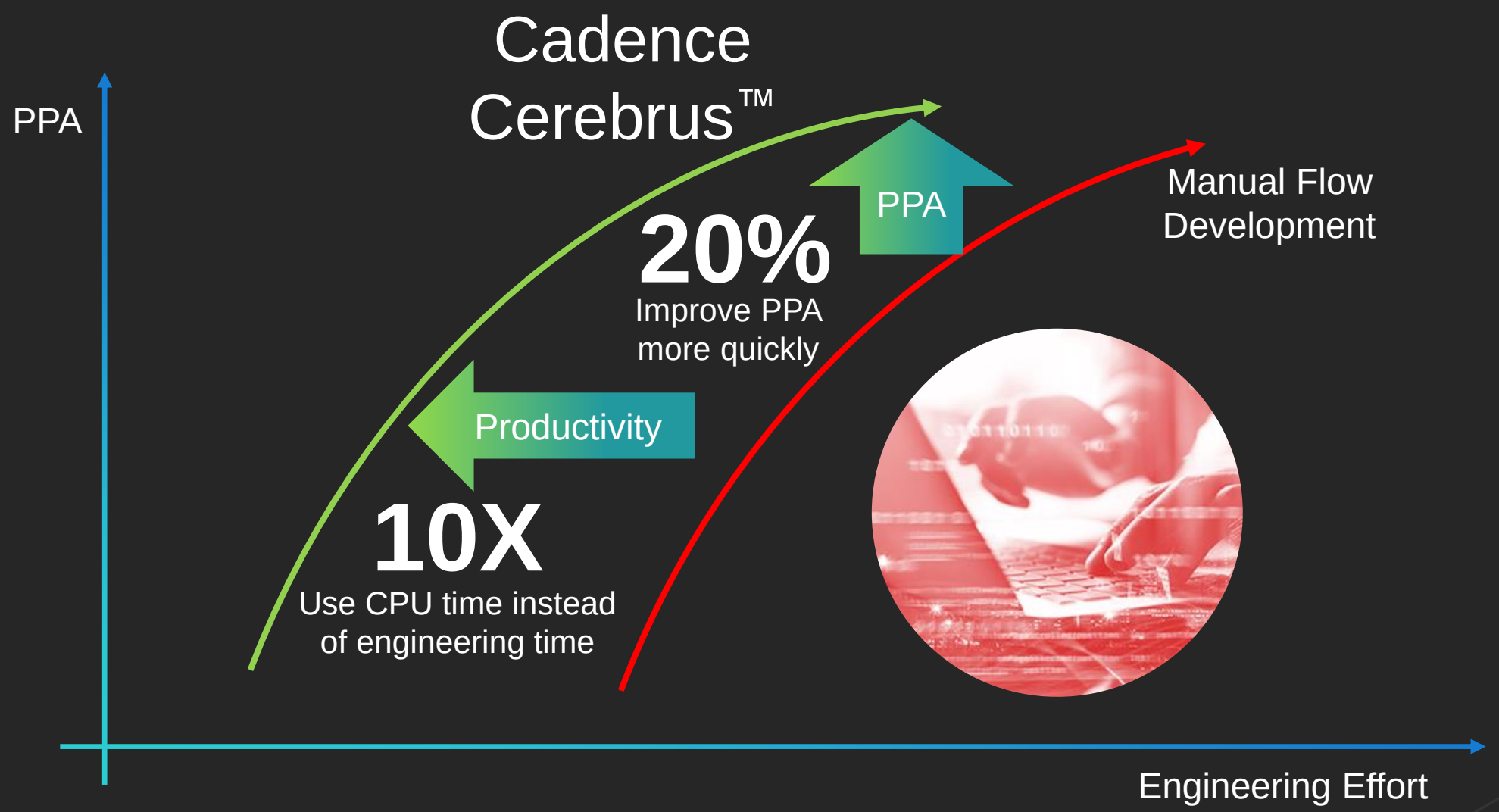
Machine Learning Inference Model

More Accurate Model

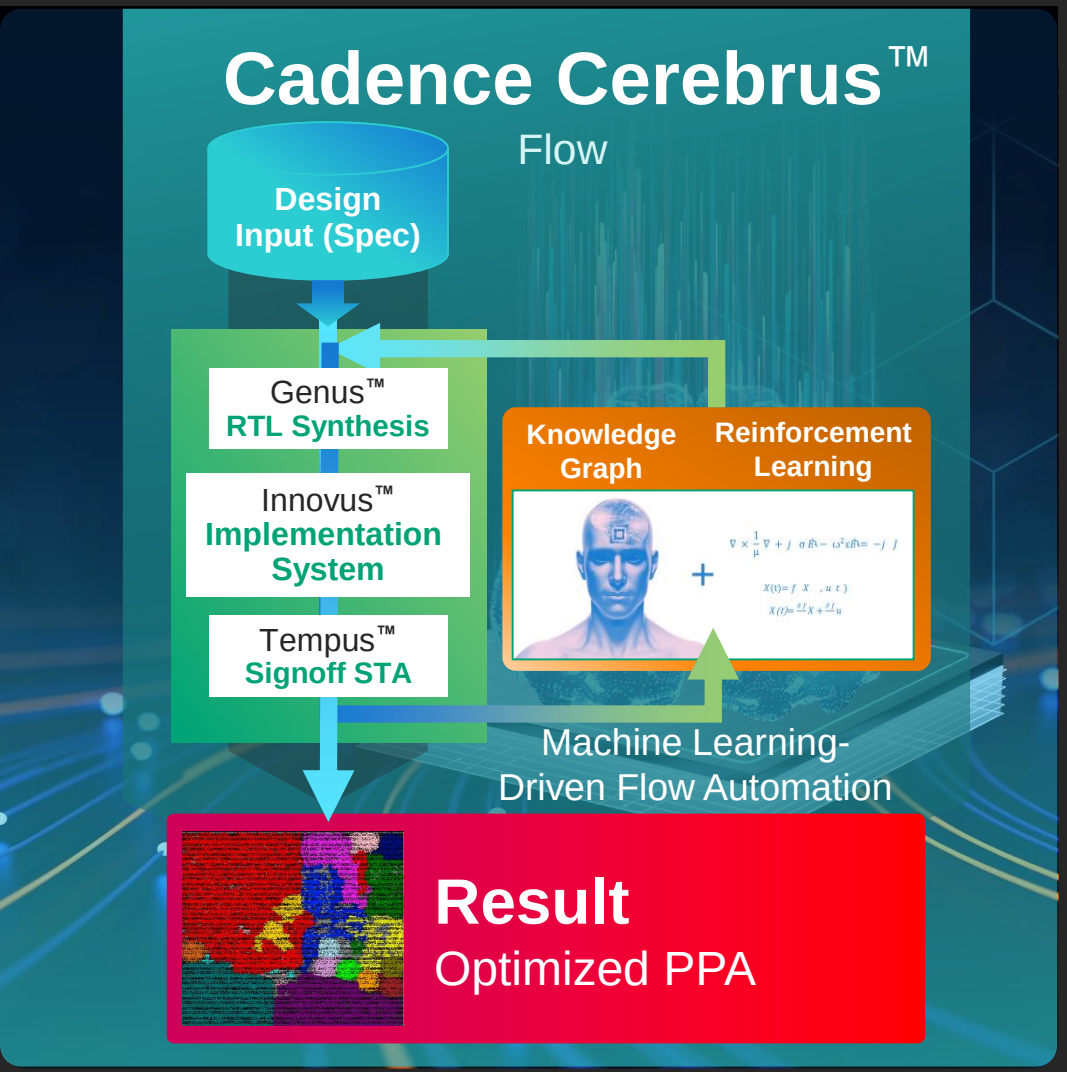
Improved Design Performance

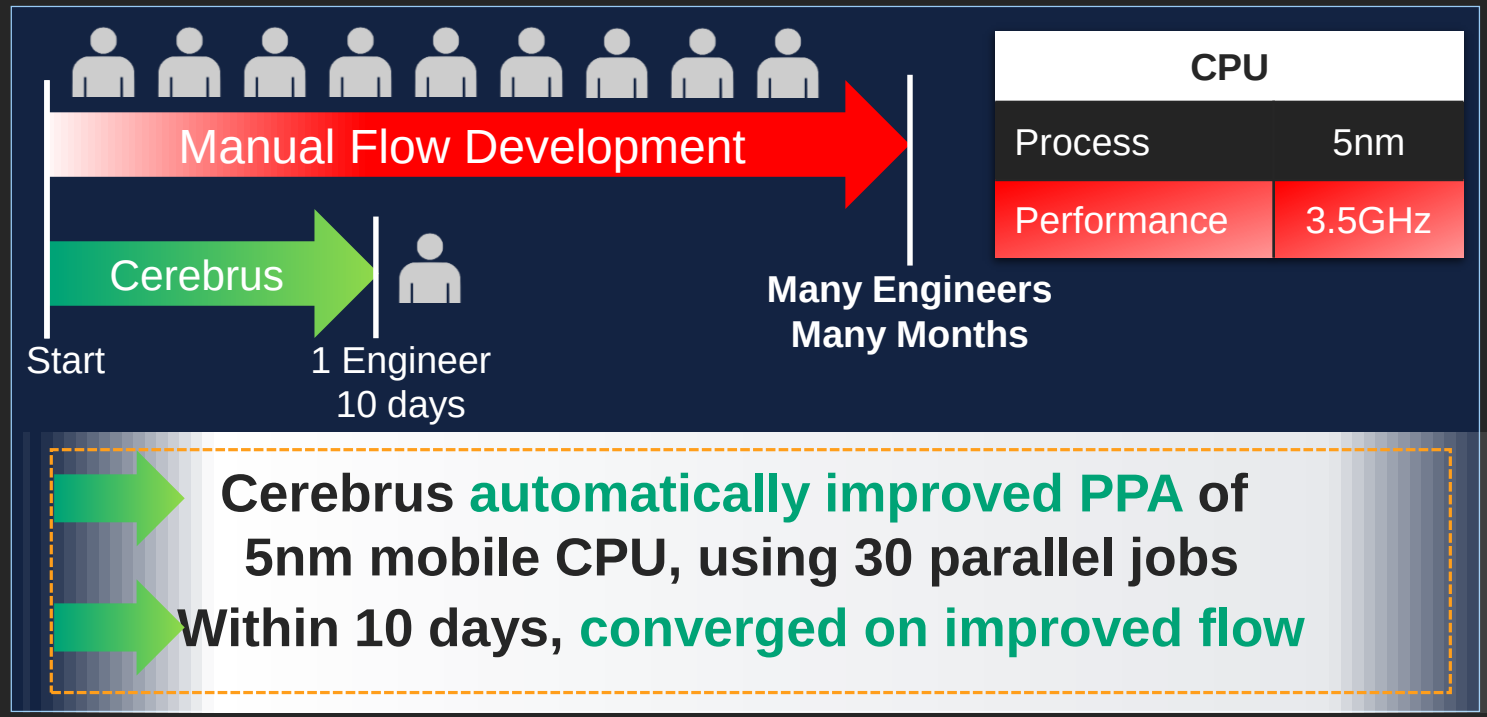
Node	WNS	TNS	Pwr
8nm	23%	67%	3.6%
7nm	5%	77%	3.4%
5nm	25%	49%	1.1%
12nm	38%	22%	1%
5nm	18%	51%	2.5%

ML Outside Objective: Improve the PPA/Productivity Curve



Cadence Cerebrus: ML for Better PPA and Full Flow Productivity





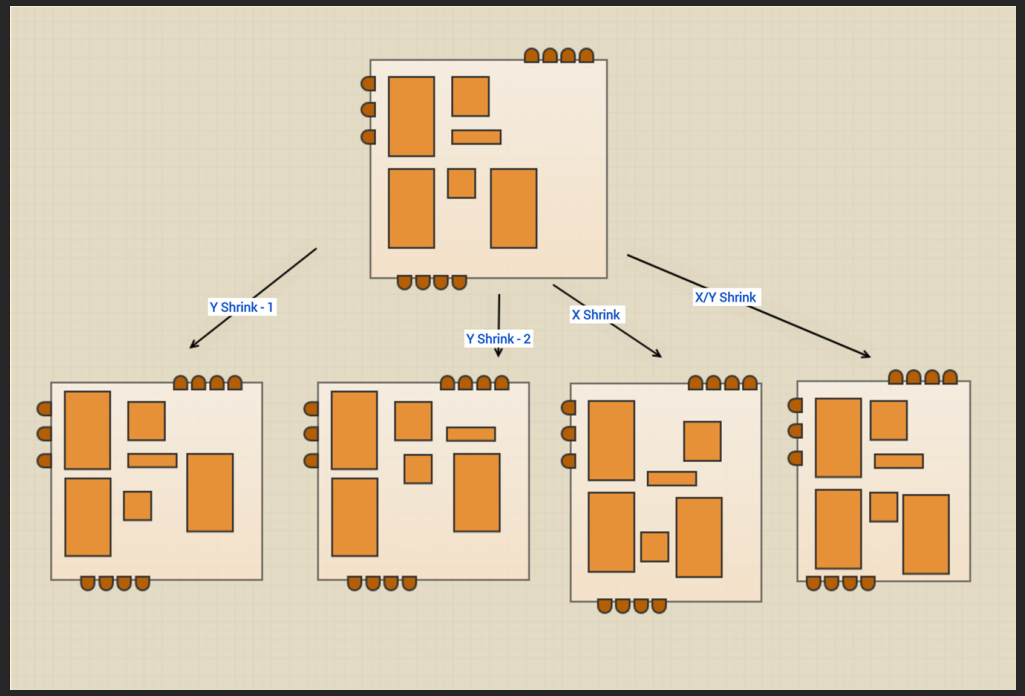
Cerebrus automatically improved PPA of 5nm mobile CPU, using 30 parallel jobs

Within 10 days, converged on improved flow

Cerebrus Improvements vs Baseline

Parameter	Improvement	Percent
Performance	420MHz	14%
Leakage power	26mW	7%
Total power	62mW	3%
Density		5%

Cadence Cerebrus: ML for Automated Floorplan Optimization



Design – CPU Core	
Process	12nm
Performance	2GHz

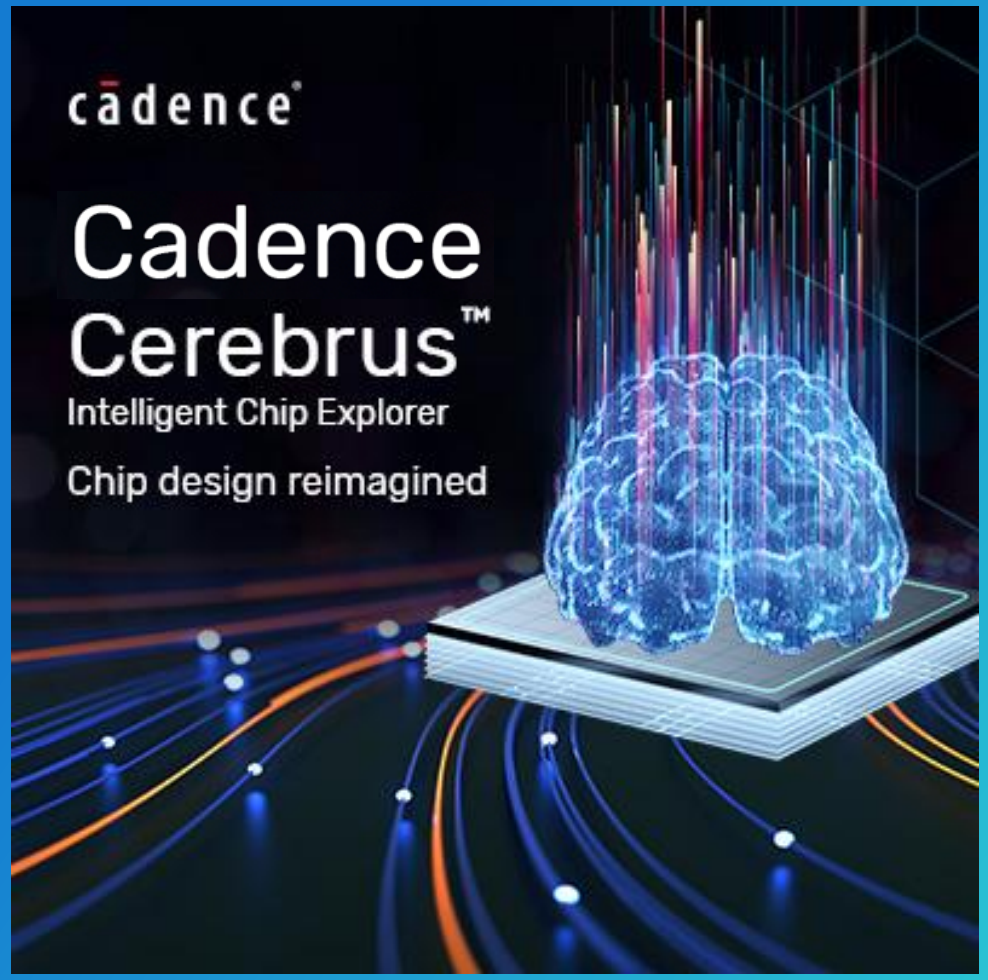
Customer wanted to achieve 2GHz on latest CPU implementation

Cerebrus optimized floorplan and implementation flow concurrently

- Floorplan can be **automatically resized in any direction**
- **Innovus™** mixed placer used to find **optimal macro location in resized floorplan**

Cerebrus Improvements vs Baseline

Parameter	Improvement
Performance	+200MHz
Total failing timing	83%
Leakage power	17%



RENESAS

To efficiently maximize the performance of new products that use emerging process nodes, digital implementation flows used by our engineering team need to be continuously updated. **Automated design flow optimization is critical for realizing product development at a much higher throughput.** Cerebrus, with its innovative ML capabilities, and the Cadence RTL-to-signoff tools have provided automated flow optimization and floorplan exploration, improving design performance by more than 10%. Following this success, the new approach will be adopted in the development of our latest design projects.

Satoshi Shibatani, director, Digital Design Technology Department, Shared R&D EDA Division, Renesas

Summary

AI/ML Productivity Improvements - Some Examples

Functional Verification	Up to **5X reduction in simulation cycles (**same coverage) Up to **4X** (2X avg.) **better out-of-the-box proofs**
Digital Implementation	Up **20% better PPA**, up to **10X productivity**
Library Characterization	**Accelerated library development** Example: 47% of libs interpolated 98%+ pass rate
Custom IC Implementation	Accurate **response surface model** of the device or block **Layout group prediction**
Design for Manufacturing	**Hotspot prediction** **In-design detection and fixing**
PCB Synthesis	**Faster design closure** **Routability**
System Design and Analysis	**Reduction in simulation time**