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Fault Testing and Diagnosis Techniques for Carbon Nanotube-Based FPGAs

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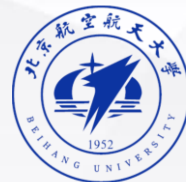


Outline

Background and Introduction of CNT-based FPGAs

- MWCNT and CNFET
- CNT-based FPGA Architecture

Ring Oscillator-based Delay Fault Testing

- The Delay Fault of MWCNT Interconnects
- RO-based Delay Fault Testing of MWCNT interconnects

Fault Testing Methodologies for Configurable Logic Blocks

- Fault model and Fault Testing for a Single CNT-based CLB
- Fault Testing for the Overall CLB Array

Experiments and Conclusion

Background

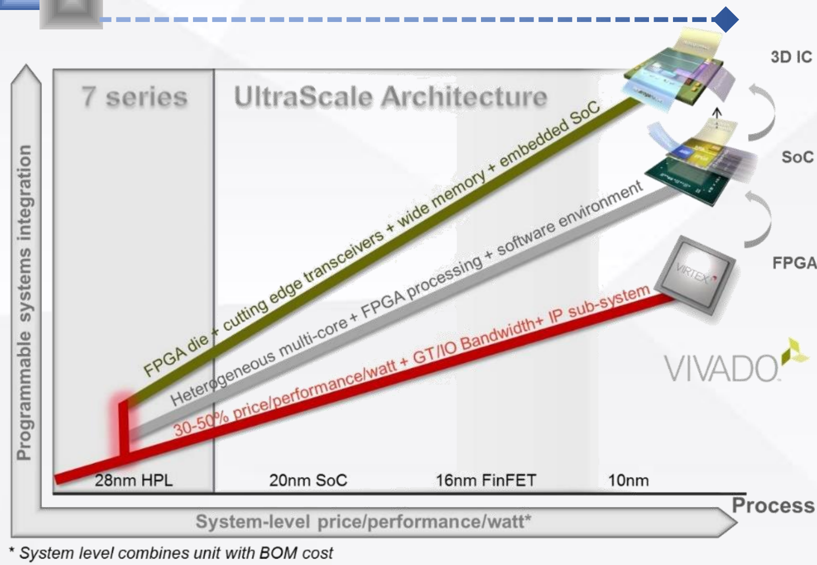
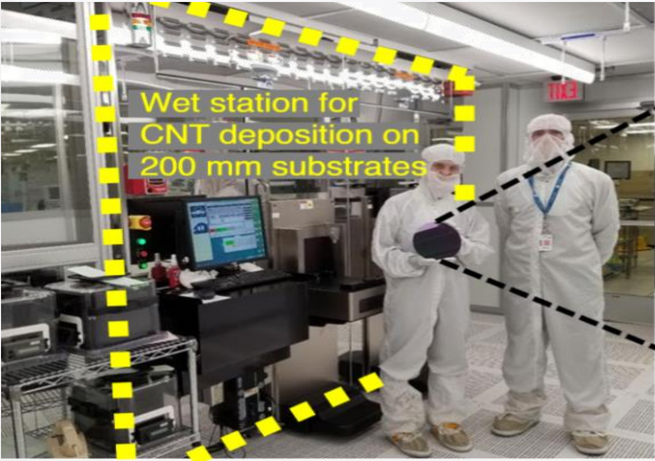
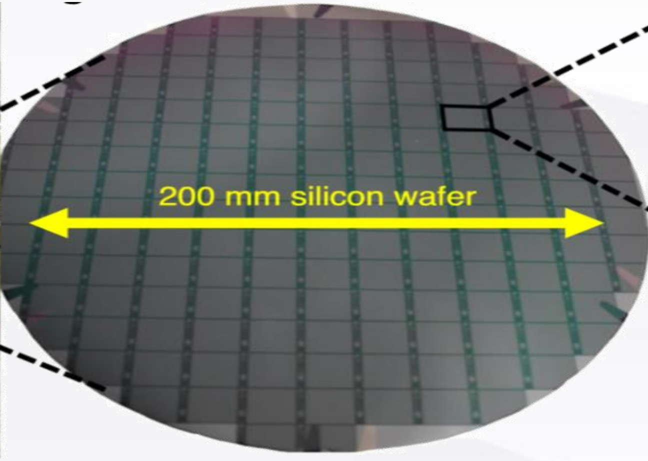


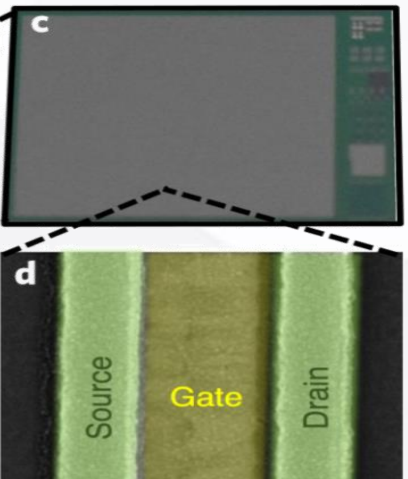
Fig. 1. The manufacuturing route of Xilinx

Technical bottlenecks of FPGAs

- Increased resistivity of Cu interconnects → Multi-walled Carbon Nanotube (MWCNT) superior conductivity and ampacity
- MOSFETs suffer from lower power efficiency → Carbon Nanotube Field Transistor (CNFET) 2 times less delay 6 times less power consumption







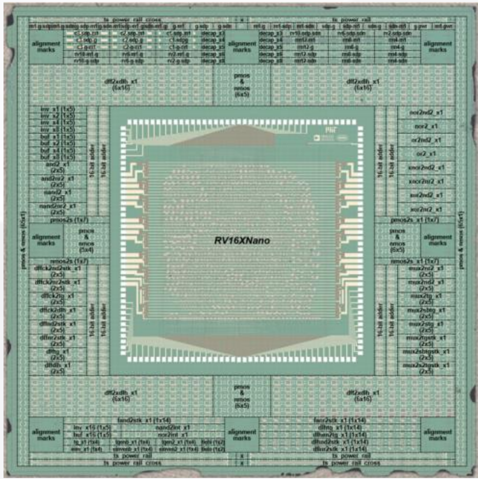


Fig. 2. (a) Integration of CNFETs; (b) a 200 mm CNFET wafer; (c) SEM image; (d) a fabricated RV16X NANO die. [1]

[1] G. Hills, *et. al*, "Modern microprocessor built from complementary carbon nanotube transistors," Nature, vol. 572, no. 7771, pp. 595-602, 2019.

Introduction to the Faulty MWCNT and CNFET

Delay Fault of CNT Interconnects

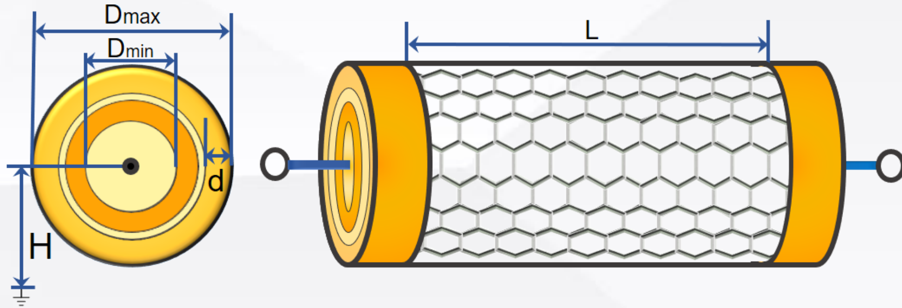


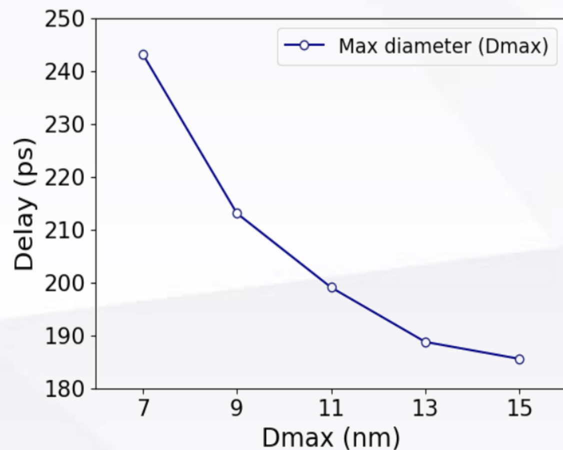
Fig. 3. Cross-sectional and 3D view of a CNT structure.

Carbon Nanotube (CNT)

- A CNT interconnect has several concentric shells

Process Variations

Dmax Variations



Chirality Variations

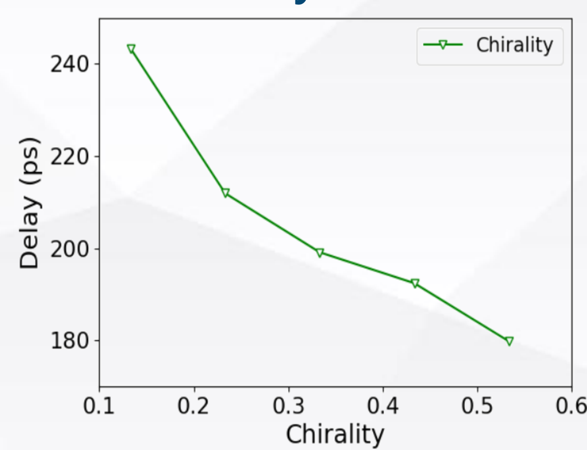


Fig. 5. The delay between two adjacent CNT-based CLBs

Shorted CNFET induced by an m-CNT

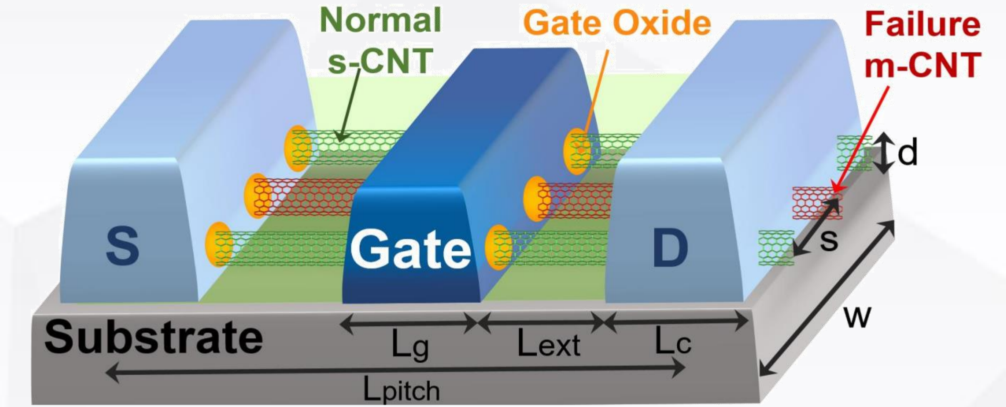


Fig. 4. 3D view of a faulty CNFET structure

CNT-based Field-Effect Transistor (CNFET)

- The structure and operation are analogous to that of a silicon-based MOSFET
- Semiconducting CNTs (s-CNTs) form the channel between the S & D contacts

Imperfect ⇩ **Fabrication Process**

- Metallic CNTs (m-CNTs) lead to a **short defect**

Introduction to the CNT-based FPGA

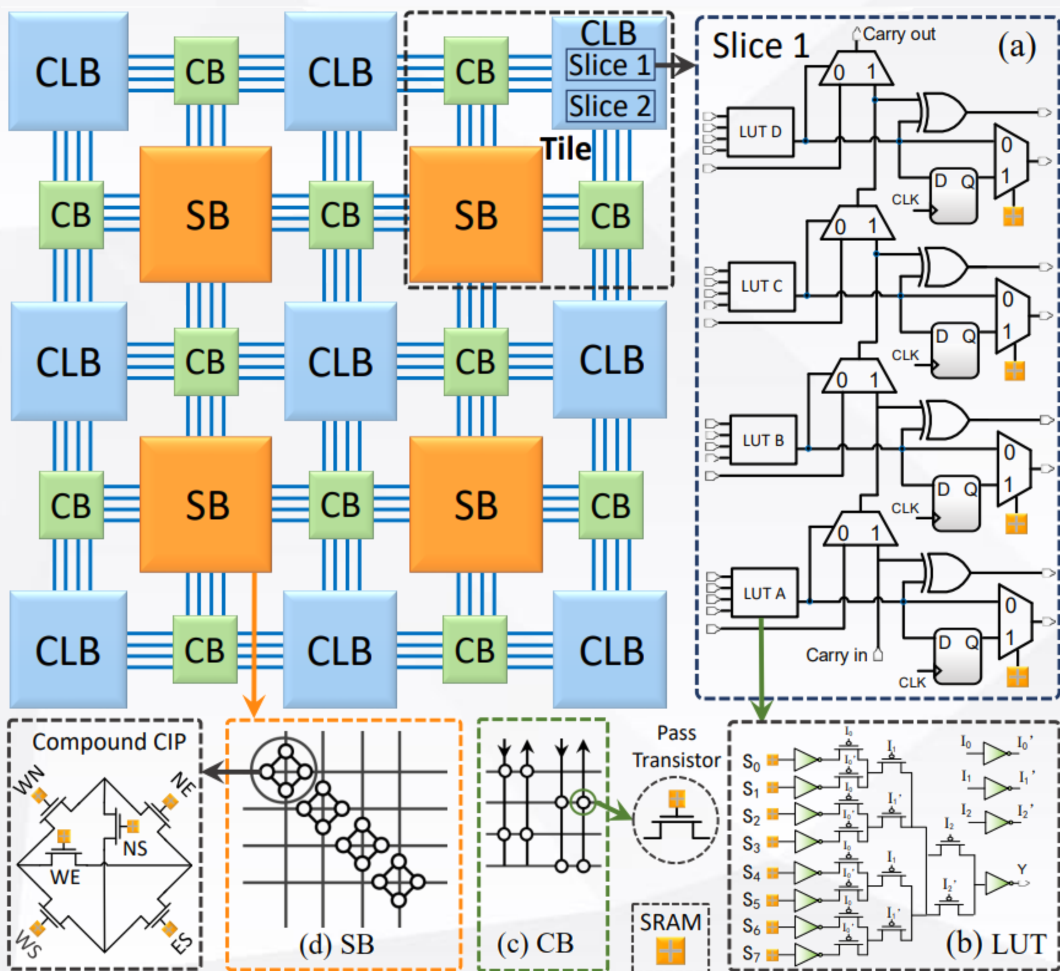


Fig. 6. The CNT-based FPGA architecture.

An Island-based Architecture

➢ **Configurable Logic Block (CLB)**

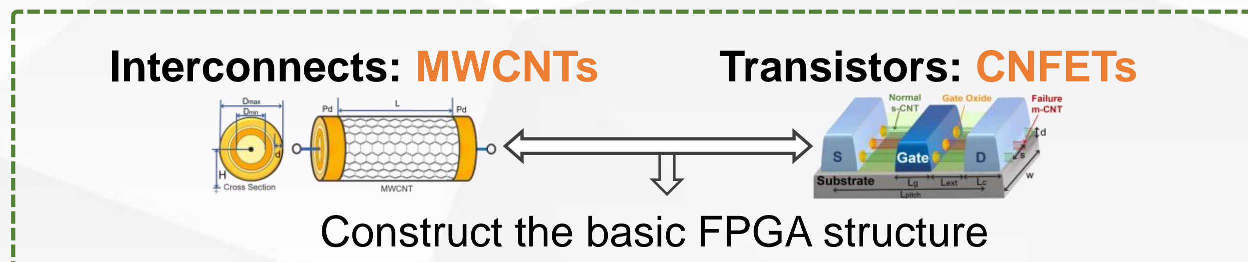
- **Lookup Table (LUT)** ⇨ **Implement Boolean functions**
  Static Random-Access Memories (SRAMs)
  Multiplexers (MUXs)
- **Carry Chain** ⇨ **Compute both the carry-out and sum bits**
  MUXs and XOR gates
- **Trigger** ⇨ **For timing output**
- **MUX** ⇨ **Select the registered output or not**

➢ **Connection Block (CB)** ⇨ **Connect channels and IO ports of CLBs**

- **Programmable Switches**
- **MWCNT interconnects**

➢ **Switch Blocks (SBs)** ⇨ **Interconnect programmability**

- **Configurable Interconnect Points (CIPs)**



[2] 7 Series FPGAs Configurable Logic Block User Guide. Accessed: 2021. [Online]. Available: https://www.xilinx.com/support/documentation/userguides/ug4747Serie-sCLB.pdf.

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The Delay Fault of MWCNT Interconnects

Monte Carlo Analysis — The delay between two adjacent CLBs considering MWCNT variations

- **The maximum diameter (Dmax)**

  A Gaussian distribution: N ~ （11nm， 1.65^2 nm^2）

- **The chirality of each shell**

  A Bernoulli distribution: each shell of ⅓ (or ⅔) probability to be metallic (or semiconducting)

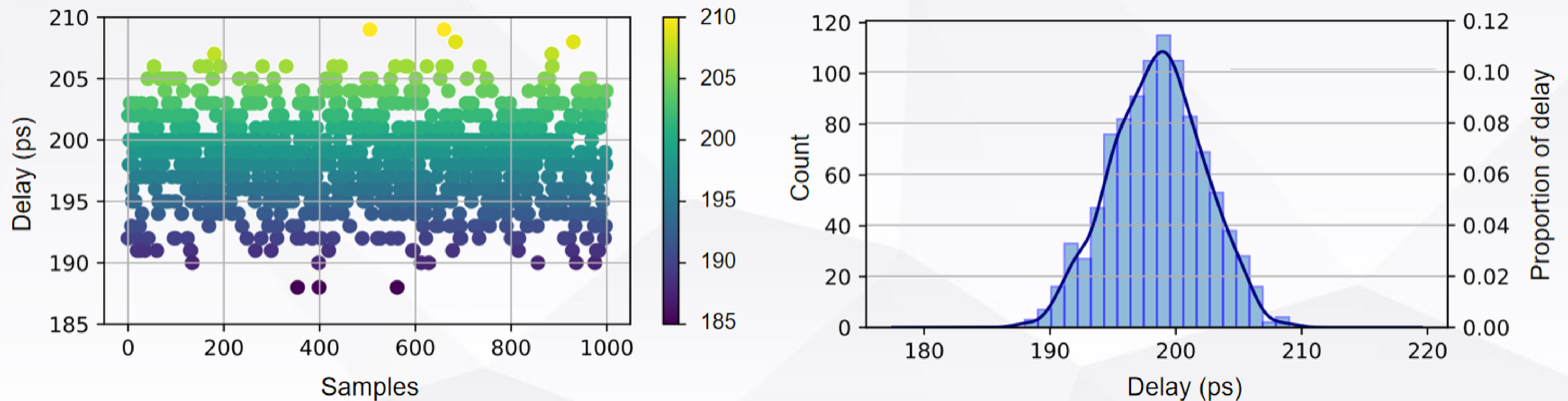

Fig. 7. The Monte Carlo simulation of the delay between two adjacent CLBs. (a) Scatter diagram. (b) Normal distribution diagram.

- A few interconnect paths exist **large delay variations**. As the FPGA fabrication technology **migrates to deep sub-micron regime**, the impact of delay faults on interconnect paths will become **more acute**.

Ring Oscillator-based Delay Fault Testing

Ring Oscillator (RO) technique is the standard method to measure delay variations of the ICs.

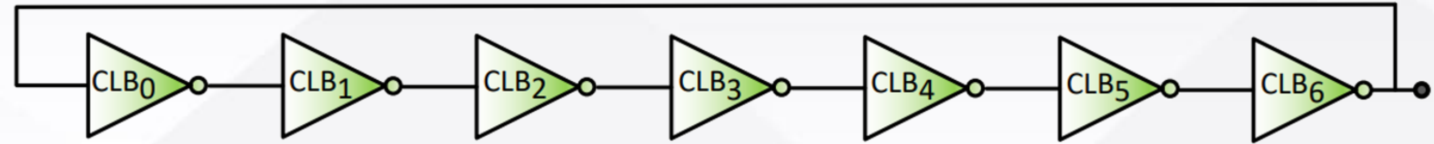

Fig. 8. The ring oscillator structure with 7-stages.

- An RO consists of an odd number of inverting logic stages connected in series to form a closed-loop chain.

An XNOR-based LUT Mapping Configuration

Table 1 Formation of oscillator paths in LUTs using XNOR logic

I0	I1	I2	I3	I4	I5 (Input)	Output = I5⊙I4⊙I3⊙I2⊙I1⊙I0
0	0	0	0	0	0	SRAM0 is mapped to value '1'
0	0	0	0	0	1	SRAM0 is mapped to value '0'

(Note that the operator '⊙' represents the XNOR operation.)

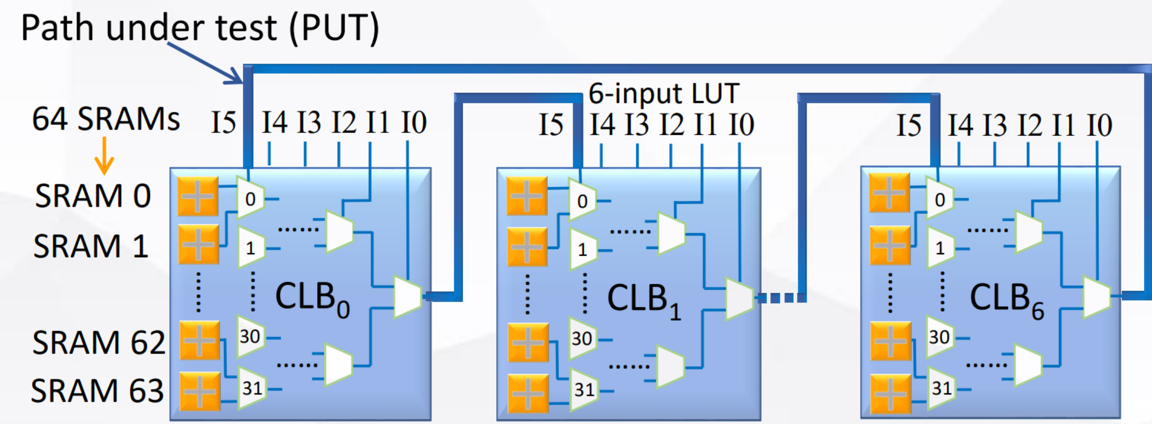

Fig. 9. Ring oscillator maps into seven 6-input LUTs

- A 6-input LUT consists of 64 SRAMs and a 64:1 MUX.
- XOR function can be realized by mapping LUTs
- The output is determined by the values of six selectors (I5 - I0)
- LUT input pin I0 serves as input to inverter logic.

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Metallic-CNT Induced Fault Model

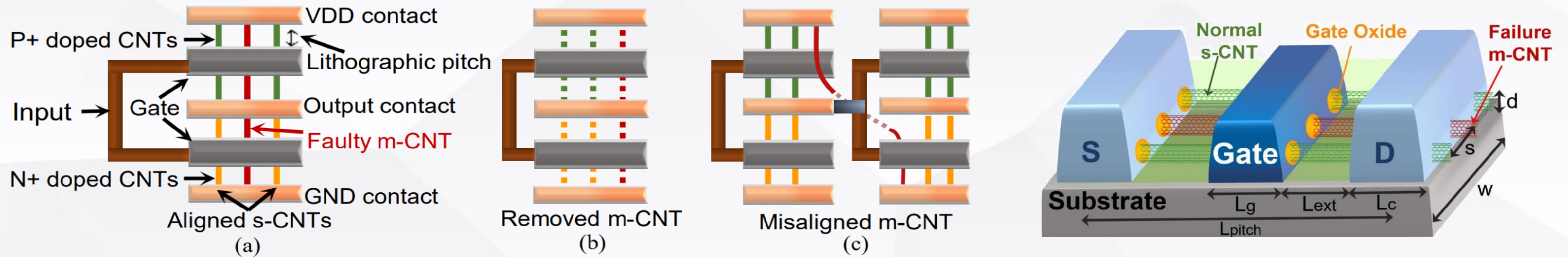
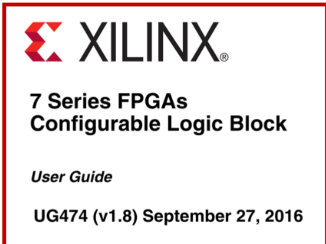


Fig. 10. (a) m-CNT leads to short inverter. (b) m-CNT removal leads to open inverter. (c) Misaligned CNTs in two-stage inverter.

- **Normal semiconducting CNTs (s-CNTs) ⇨ promising channel materials**
- **A typical CNT synthesis process ⇨ 3%-33% m-CNTs, leading to a short defect**
- **The m-CNT removal process may lead to the removal of s-CNTs under the FET**

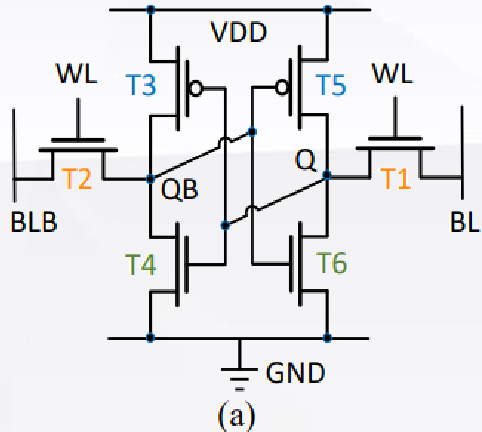
- **CNT length variation：** CNT may terminate at any place in the catalytic
- **Misaligned CNTs：** CNT grows at an inclined angle

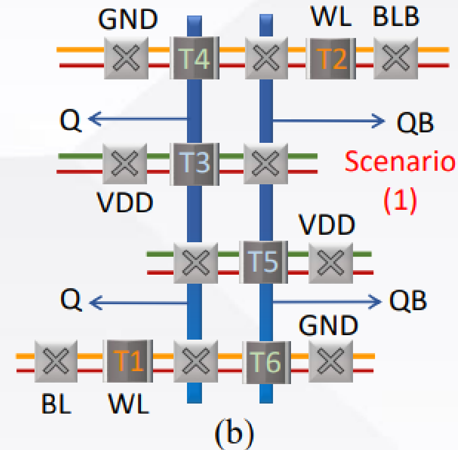


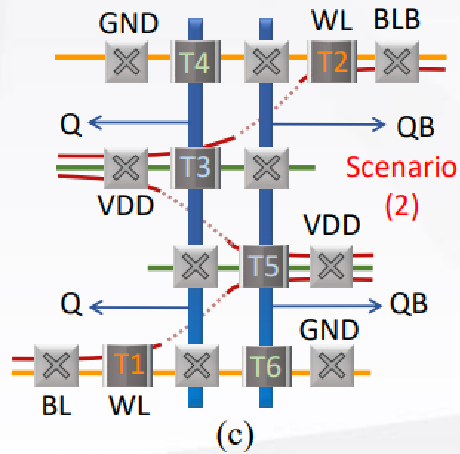
- **According to the Xilinx 7 Series User Guide, the CLB mainly contains SRAMs, multiplexers, D flip-flops and carry chains**
- Next, detailed fault modeling is performed for SRAM and MUX.

SRAM Fault Model

CNT interconnect | Contact | Gate Mental | Failure m-CNT
s-CNT for P-CNFET | s-CNT for N-CNFET | Etched m-CNT







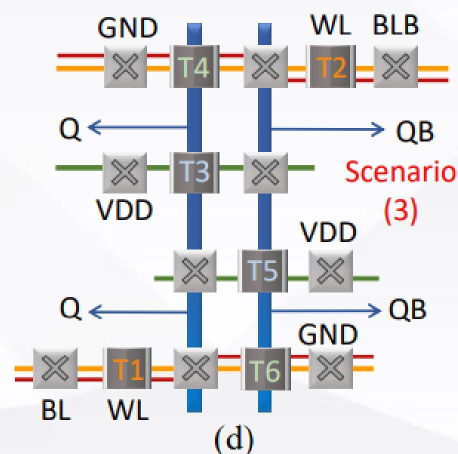


Fig. 11. (a) The circuit schematic of CNT-based SRAM. (b) The faulty layout of SRAM induced by m-CNTs, which grow together with s-CNTs. (c) The faulty layout of SRAM induced by misaligned m-CNTs. (c) The faulty layout of SRAM due to the length variation of m-CNTs.

Faulty Scenarios:

(1) an m-CNT passes through two horizontal CNFETs in a row

(2) a misaligned m-CNT affects two CNT bundles

(3) an m-CNT terminates after it passes through one CNFET

All the fault types can be considered as the Stuck-At Faults

TABLE II
THE FAULT MODELS OF CNT-BASED SRAM.

The growth of m-CNT	Short Fault (X-Y) between two points (VDD → 1, GND → 0)	Scenarios Position	SRAM Fault Model
(1) A row of m-CNTs grow together with s-CNTs	Q-0, QB-0	T1, T6	Stuck-at 0
	Q-0, QB-0	T2, T4	Stuck-at 0
(2) Misaligned m-CNT in a SRAM	Q-1, QB-1	T2, T3	Stuck-at 1
	Q-1, QB-1	T3, T5	Stuck-at 1
	Q-1, QB-1	T1, T5	Stuck-at 1
(3) m-CNT with length variation, and only affect one CNFET	Q-BL/Q-1	T1/T3	Stuck-at 1
	QB-BLB/Q-0/QB-1	T2/T4/T5	Stuck-at 0
	Q-0, QB-0	T6	Stuck-at 0

Multiplexer Fault Model

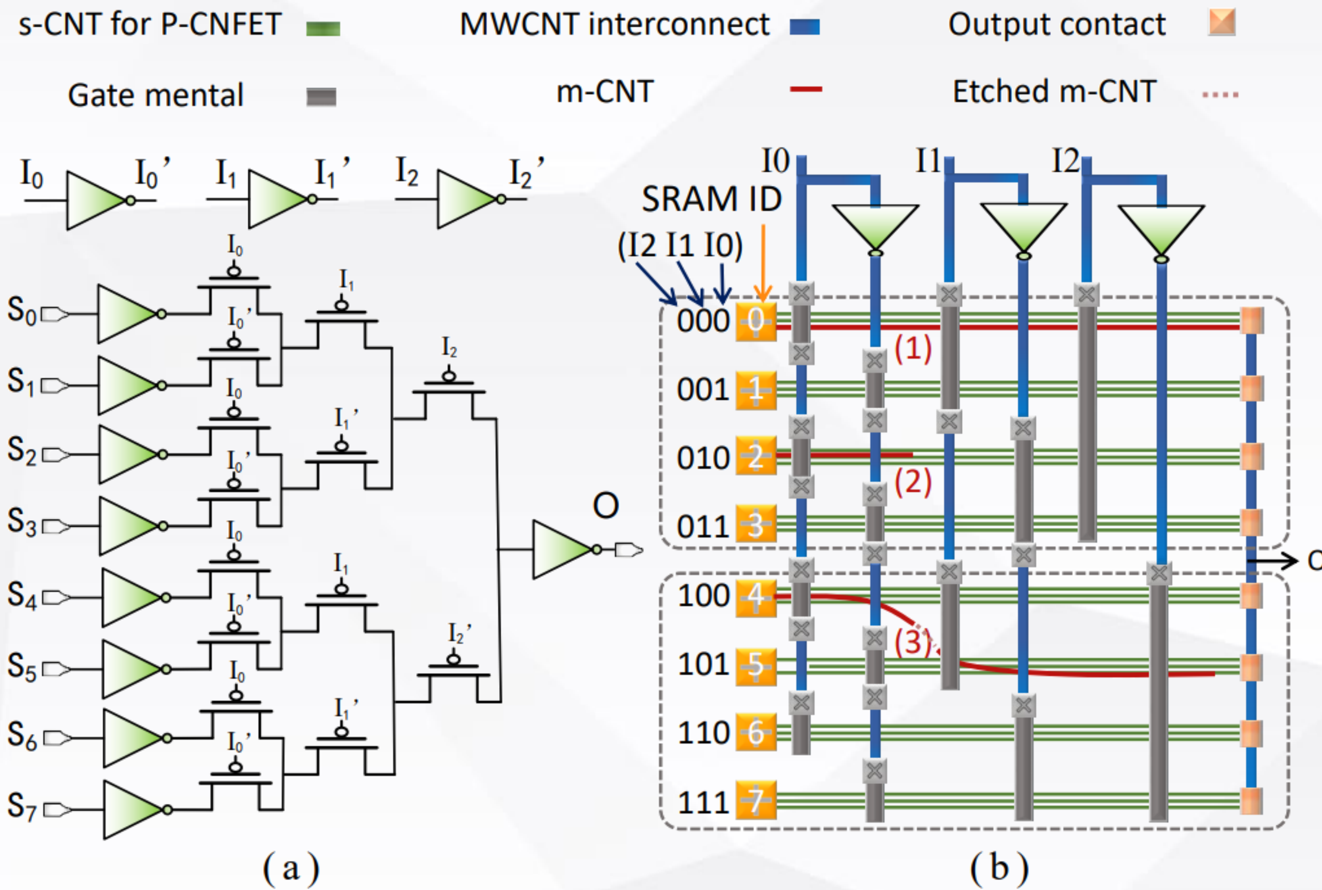


Fig. 12. (a) The circuit schematic of MUX. (b) The faulty layout of MUX induced by m-CNTs.

An m-CNT passes through a whole row

Short between SRAM-0 and output

An m-CNT terminates after passing one I signal

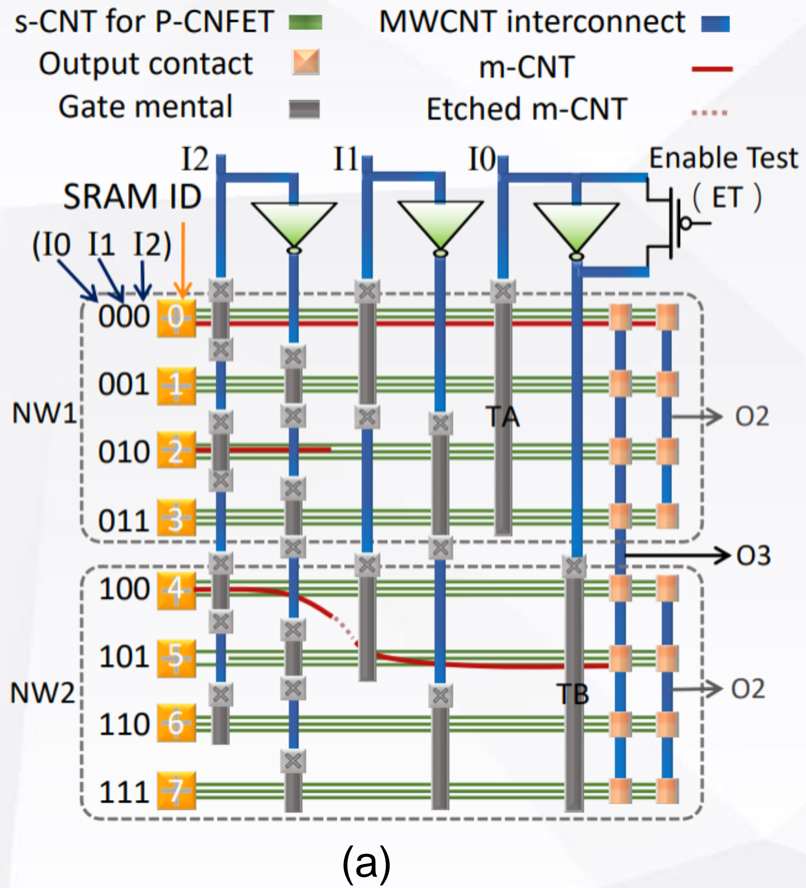
Short between SRAM-2 and a transmission gate

When the SRAM-3 output is selected, it causes a wired-AND/OR fault of the values stored in SRAM-2 and SRAM-3.

A misaligned m-CNT affects two CNT bundles

Affect the output of SRAMs corresponding to $\overline{I2}$

Fault Testing for a Single CNT-based CLB



(a)

ET=0	Configuration			
I0=0	C1	C2	C3	C4
S0	0	0	0	1
S1	0	0	1	1
S2	0	1	0	1
S3	0	1	1	1
S4	1	0	0	0
S5	1	0	1	0
S6	1	1	0	0
S7	1	1	1	0

1st
2st
3st
4st

(b)

Design Improvement：

- A P-CNFET is placed on the right of the inverter connected with the selected signal I2
  - ET=1 ⟹ Normal Mode
  - ET=0 ⟹ Test Mode
- Test two networks (NW1 and NW2) in parallel

Fig. 13. (a) The proposed improved design of LUT. (b) The traditional test configuration scheme.

[3] S. K. Lu, *et. al*, “Fault Detection and Fault Diagnosis Techniques for Lookup Table FPGAs,” VLSI Design, vol. 15, pp. 397-406, 2012.

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Fault Testing Technique for the Overall CLB Array

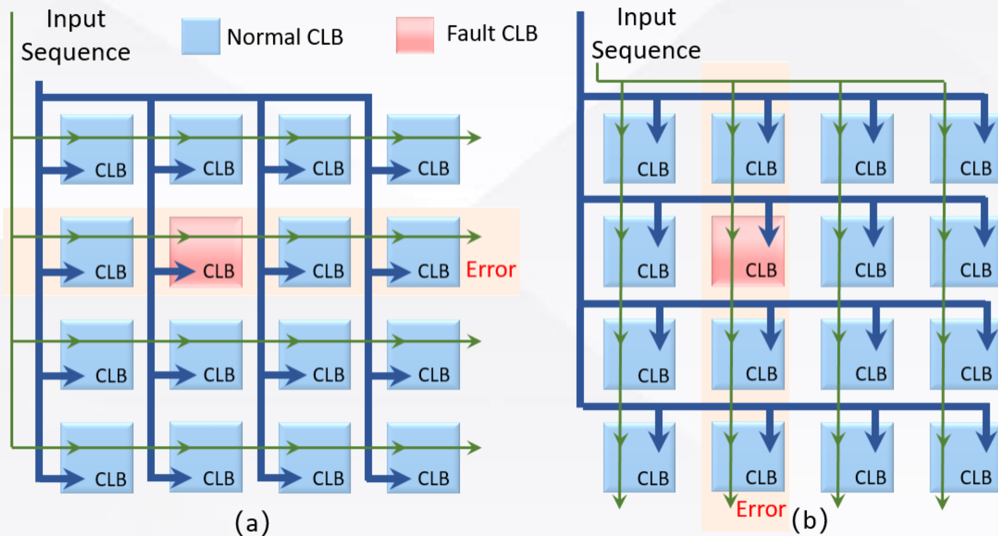
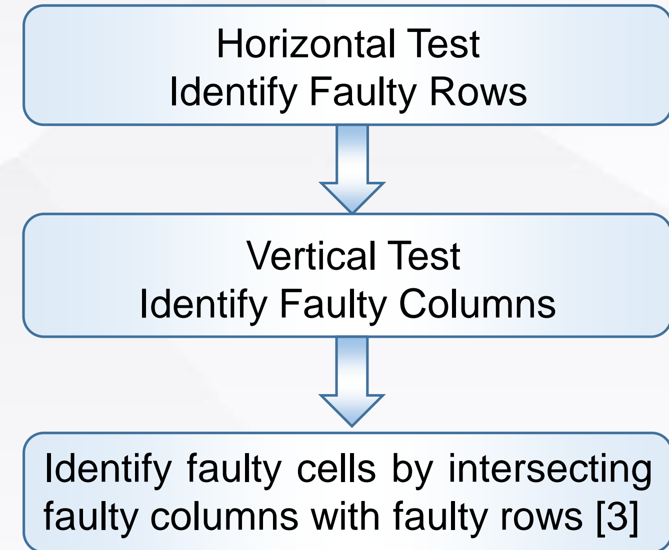


Fig. 14. The traditional method to diagnosis the faulty CLBs.



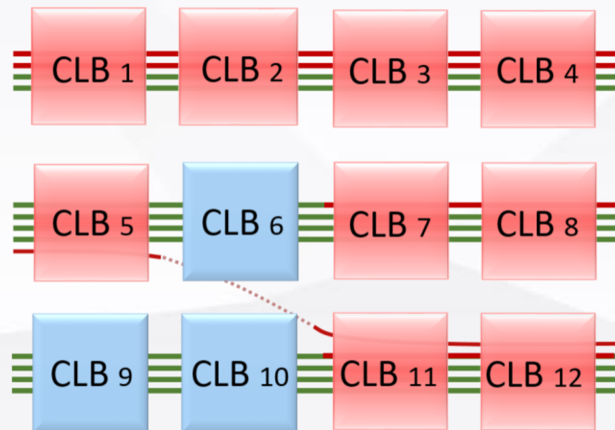


Fig. 15. The cascaded CNT-based CLBs.

- The traditional diagnostic technique cannot test the cascaded faulty CNT-based CLBs effectively

[4] T. Inoue, *et. al*, "Universal fault diagnosis for lookup table FPGAs," IEEE Design & Test of Computers, vol. 15, no. 1, pp. 39-44, 1998.

Fault Testing Technique for the Overall CLB Array

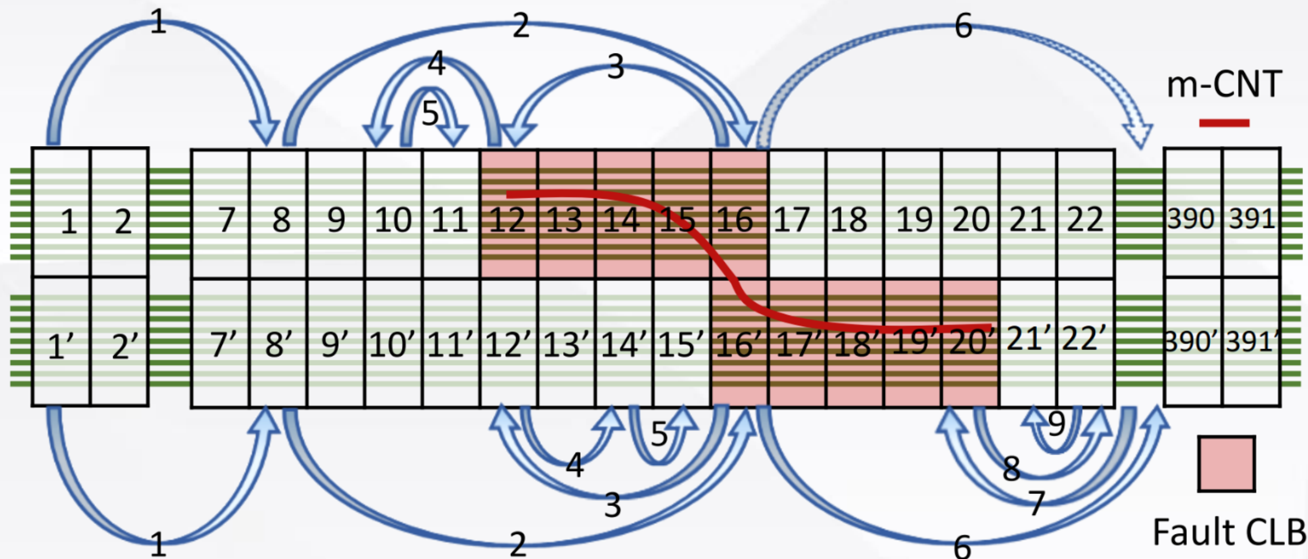


Fig. 16. Examples illustrating recursive jump test.

Algorithm 1 Recursive Test

Input:

Output: Recursive(Dir, $Step$, Key, $C_{i,j}$)

1: **if** $Step$ = 1 **then**
2: Return;
3: **else**
4: $Step$=$Step/2$;
5: Key = ($C_{i,j}$ xor $C_{i,j+Dir\times Step}$) and Key
6: **if** Key = 1 **then**
7: Dir = -Dir;
8: Recursive(Dir, $Step$, Key, $C_{i,j+Dir\times Step}$);
9: **else**
10: Recursive(Dir, $Step$, Key, $C_{i,j+Dir\times Step}$);
11: **end if**
12: **end if**

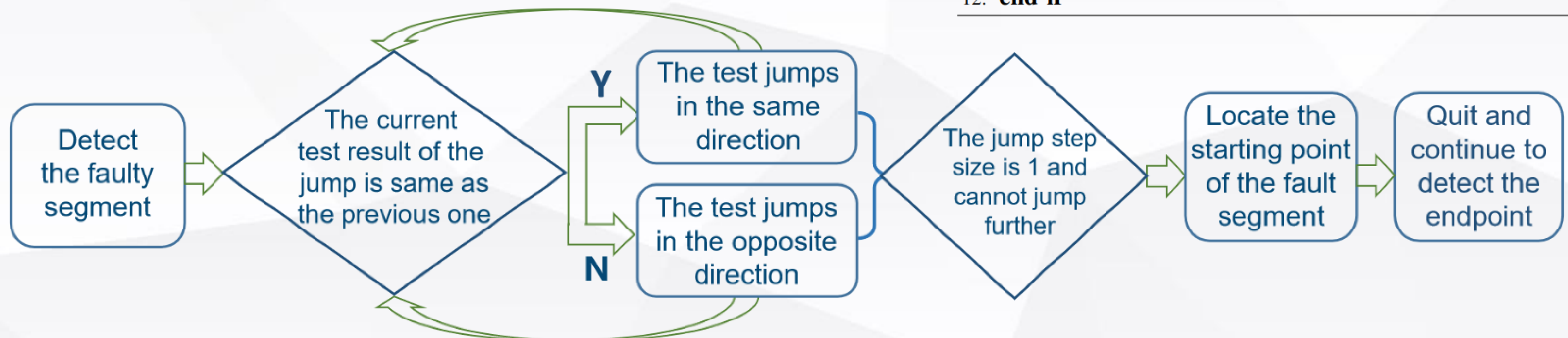


Fig. 17. Flow chart of algorithm.

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Experiments

Experimental Setup

- A basic island-style **CNT-based CLB** was built in **Simulation Platform**
- We built a simulator with the layout information of the CNT-based FPGAs in Python
- We performed **Monte-Carlo simulations** to generate 1000 basic samples of the CNT-based FPGAs, deriving the corresponding fault maps

Table IV CNFET Parameters

Definition	Value
Technology node	7nm
Transistor length: L_{pitch}	35nm
Transistor Width: W	63nm
Physical gate length: L_g	10nm
Contact length: L_c	10nm
Gate hight: H_g	15nm

Table V MWCNT Parameters

Definition	Value
Distance between MWCNT and GND: H	1μm
Portion of metallic shells: Pim	1/3
Portion of semiconducting shells: Pis	2/3
Number of shells: k	16
Outermost diameter of each CNFET: Mean-Dμ, Variation-Dσ	Dμ=11nm Dσ=1.65^2nm^2

Table VI CNT Parameters

Definition	Value
The number of CNTs for each CNFET: Mean-Nμ, Variation-Nσ	Nμ=4, Nσ=1
Probability of m-CNT: Pm	3%~33%
Probability of removed m-CNT: Prm	99.99%
Probability of removed s-CNT: Prs	5%
The angle of CNTs: Mean-Aμ, Variation-Aσ	Aμ=0°, Aσ=10°
The length of CNTs: Mean-Lμ, Variation-Lσ	Lμ=150um, Lσ=3.33um

[5] R. Chen, *et. al,* " Variability Study of MWCNT Local Interconnects Considering Defects and Contact Resistances—Part I: Pristine MWCNT," IEEE TED, 2018.
[6] Patil N, *et. al,* " Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits," IEEE TCAD, 2008.

Experiments

The Delay Fault Testing of MWCNT Interconnects

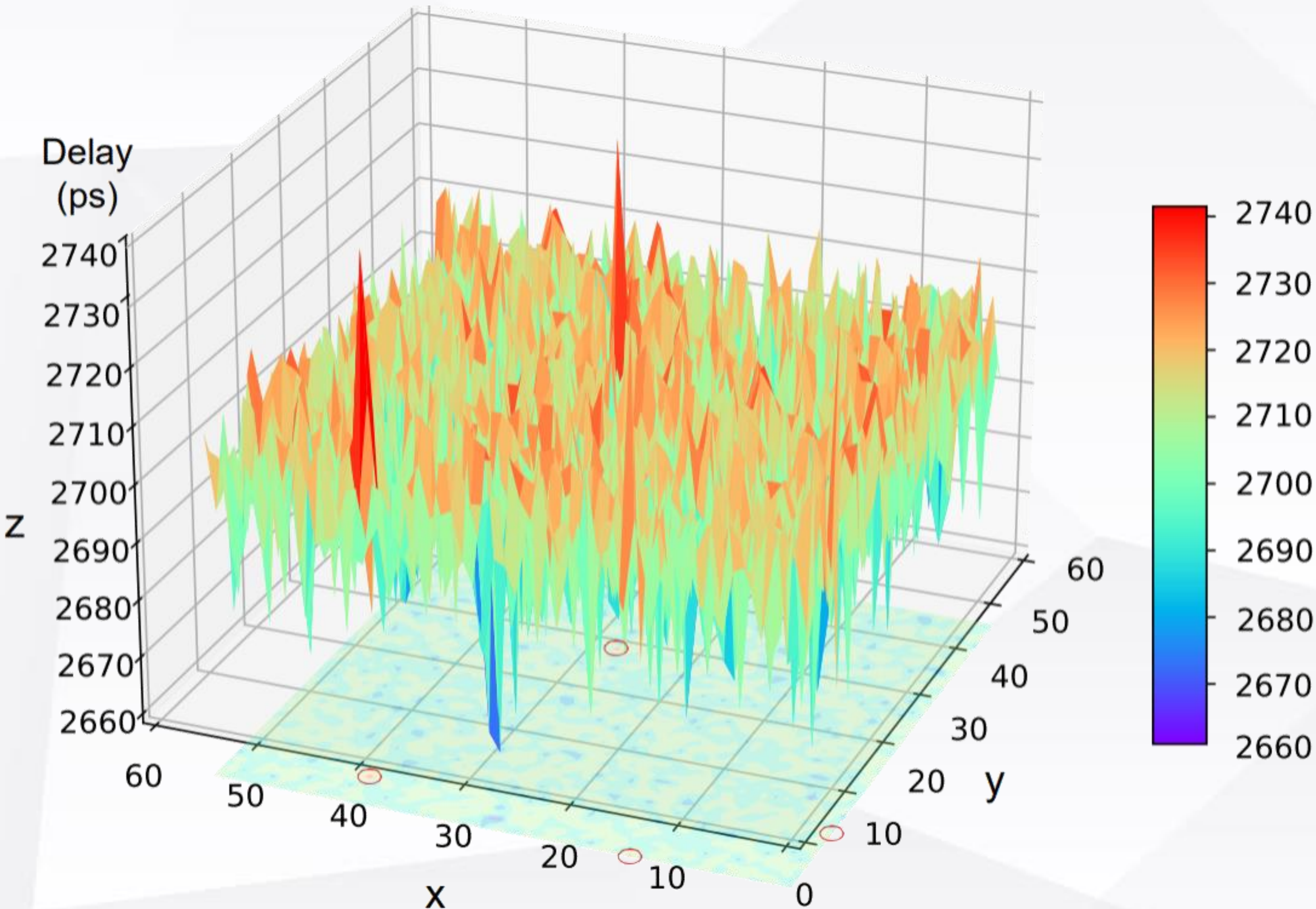


Fig. 17. The observed oscillation delay in a CNT-based FPGA.

Experimental Setup

- ROs were mapped to the LUT by the XNOR configuration
- To avoid the measurement noise, each frequency was measured three times and the average value was taken

Result

- The **mean** and **variation** of oscillation delay were **2.70ns**, **100ps**
- A few ROs with large loop delays, which seriously affect the performance of a CNT-based FPGA operating at hundreds of MHz

Experiments

Testing Overheads for m-CNT Faults in CLBs

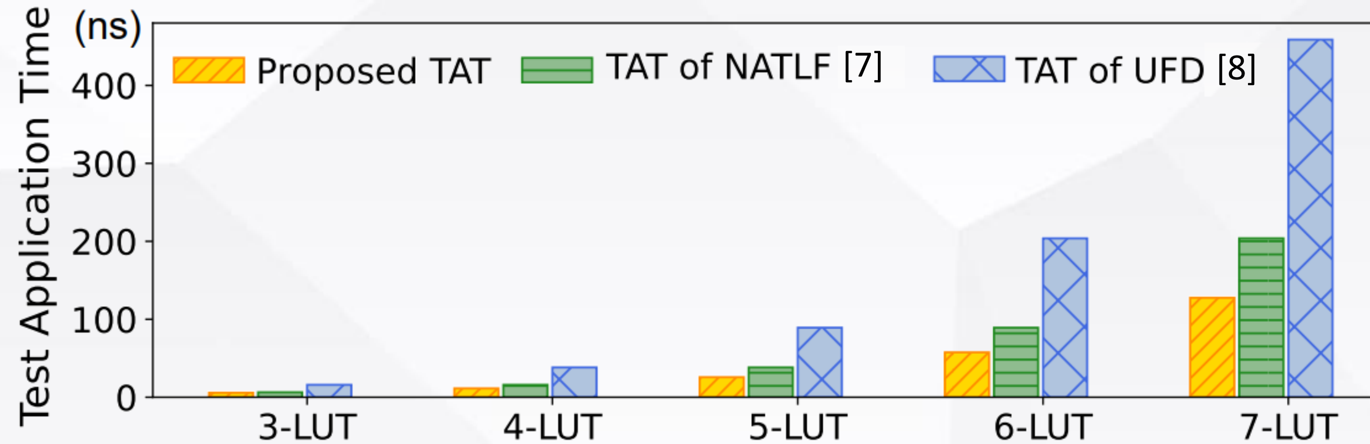
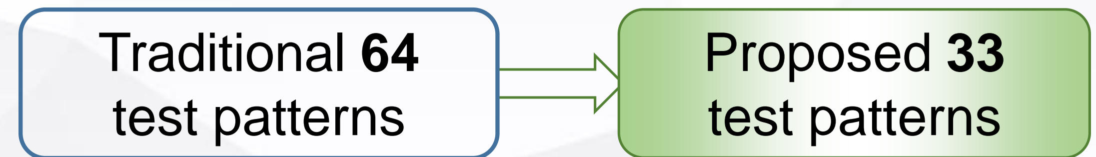


Fig. 18. Simulation results for the test application time (TAT) of different CNT-based LUTs.

- We applied the technique to a single CNT-based CLB constructed by different input LUTs
- The test application time of the proposed technique is less than the other two traditional methods

Design Improvement



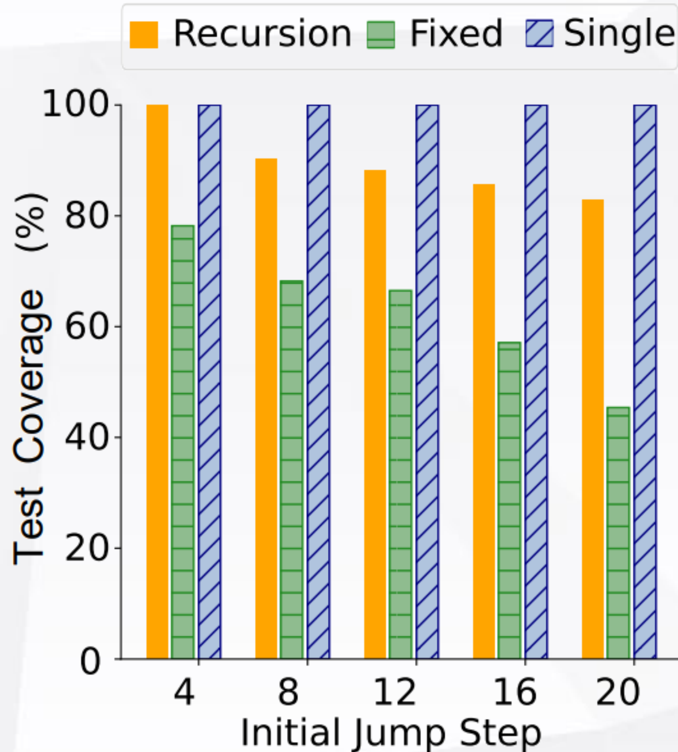
For the common 6-input LUT, the test application overheads were **reduced by 35.49%**

[7] S. K. Lu, *et. al*, "Fault Detection and Fault Diagnosis Techniques for Lookup Table FPGAs," VLSI Design, vol. 15, pp. 397-406, 2012.
[8] T. Inoue, *et. al*, "Universal fault diagnosis for lookup table FPGAs," IEEE Design & Test of Computers, vol. 15, no. 1, pp. 39-44, 1998.

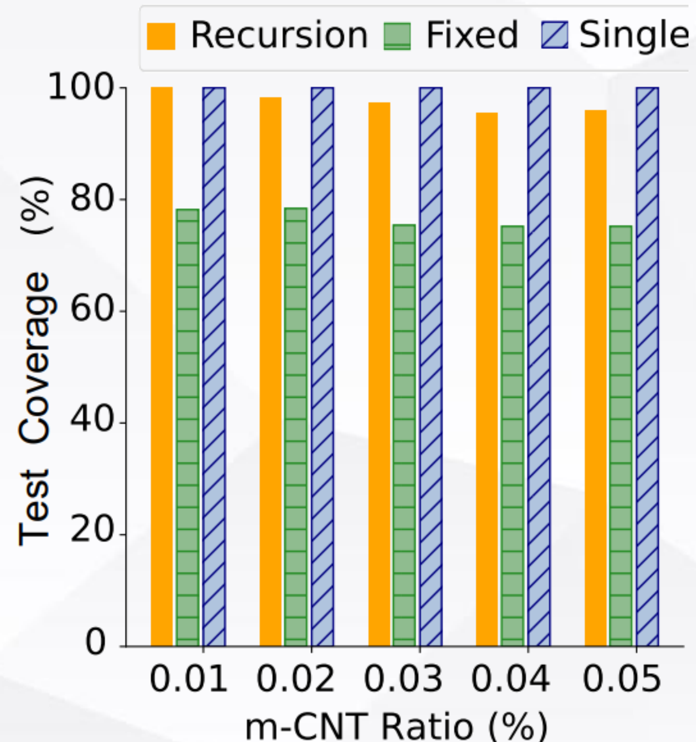
Experiments

Evaluations for testing the Cascaded Faulty CLB Segment

- Test Coverage: The percentage of all faulty cells in an FPGA array that has been identified by the jump testing



(a)



(b)

Fig. 19. Results on test converage with varing (a) jump step, (b) m-CNT ratio.

Fixed-Step Jump Test

- Lower test coverage as the initial jump step increases

Single-Step Jump Test

- Test coverage maintains at 100%

Recursive Jump Test

- The tests with **step size 4** show **100%** test coverage
- It provides **higher test coverage** than the fixed-step jump test as the initial jump step and m-CNT ratio increases

Experiments

Evaluations for testing the Cascaded Faulty CLB Segment

- Test overheads: The test overheads of the jump steps applied to the CNT-based FPGA

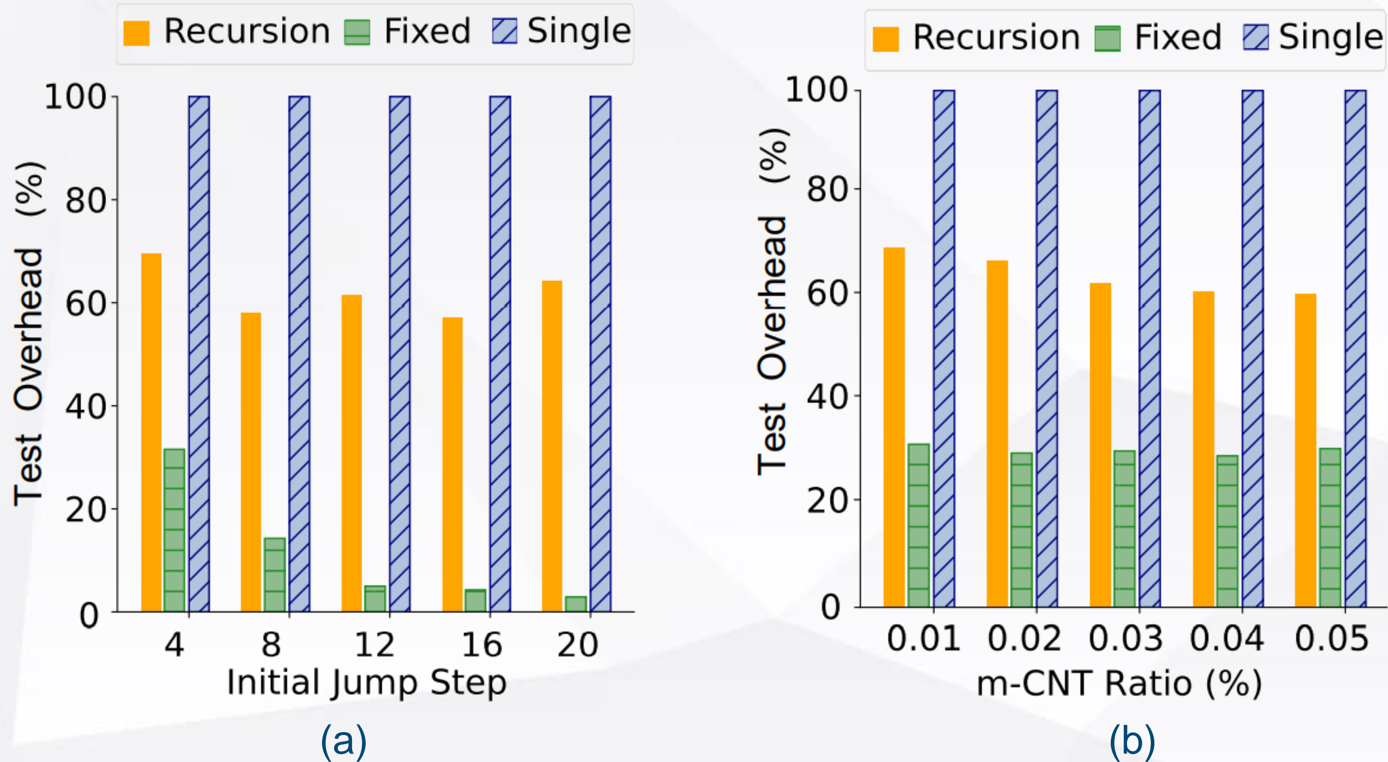


Fig. 20. Results on test overheads with varing (a) jump step, (b) m-CNT ratio.

Recursive Jump Test

- The test overheads of the recursive test decreases with the increase in m-CNT ratio.

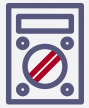
An interesting phenomenon

- The test overheads with jump step size 12 is higher than that with jump step size 8.
- Similar results can be observed with the initial jump step size 16 and 20

Compared with the single-step test, the test overheads of recursive test can be reduced **35.78%** on average.

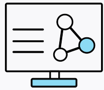
Conclusion

- Due to the imperfect fabrication process, CNT-based FPGA may exhibit unique faulty patterns



- Mapping the ring oscillator design on FPGA ⇨ Detect the delay fault of MWCNT interconnects

- An LUT-based improved design is also proposed to speed up the fault test



- The proposed testing and diagnosis techniques can achieve higher test coverage and reduce the testing overheads by 35.78%

Thanks for Your Attention!