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GS-IMTR

Graduate School
Intelligent Methods for Test and Reliability



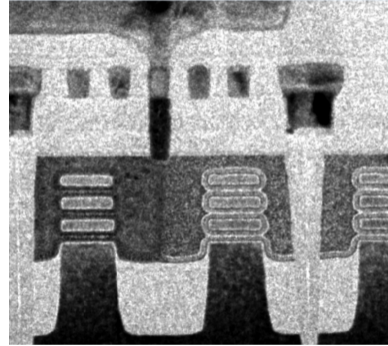
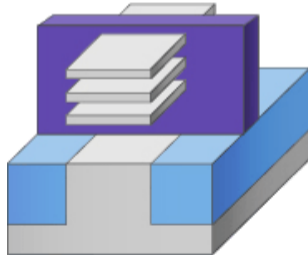
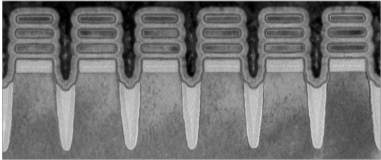
Design Close to the Edge for Advanced Technology using Ma- chine Learning & Brain- Inspired Algorithms

Hussam Amrouch, Florian Klemme,
and Paul R. Genssler

Scaling in Advanced Technology

- Transistor Technology close to fundamental limit
- TSMC 3 nm FinFET, 2 nm Nanosheet by IBM
- Less power, less area, higher clock speed, ...

→ But does your mobile run 30 % longer?

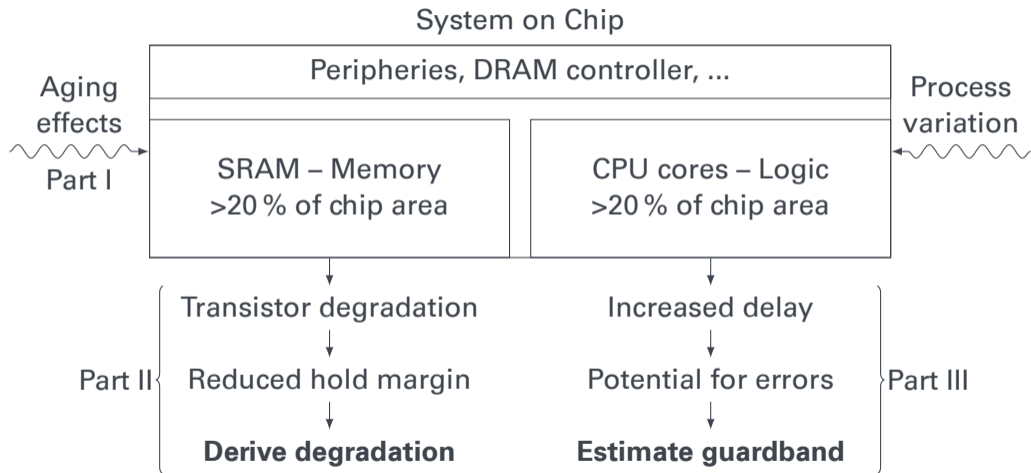


Challenges with Advanced Technology

- Increased impact of degradation
- Increased variability due to quantum effects
- Increased demand for reliable chips
- SPICE simulations are expensive
- Assumption: Transistor model available
- Diminishing returns of scaling

→ Move circuit design **close to the edge**

Our Multi-Level Approach



Background: Degradation

Design-time degradation

- key contributor: variation
- source: manufacturing
- Gaussian distribution
- constant over lifetime

Run-time degradation

- key contributor: aging (BTI, HCI)
- source: usage of circuit
- workload-dependent
- changes over lifetime

→ change in electrical properties, most importantly ΔV_{th}

→ **efficient guardband design** – small yet sufficient

Background: Concept of Hyperdimensional Vectors

- Random integer vectors A, B of dimension d
- Compute Cosine similarity $\cos(A, B)$
- Bundle multiple vectors as a set
- Bind vectors together

$$A = \begin{matrix} 0 & 1 & 0 & 1 \end{matrix}$$

$$B = \begin{matrix} -1 & -1 & 1 & 1 \end{matrix}$$

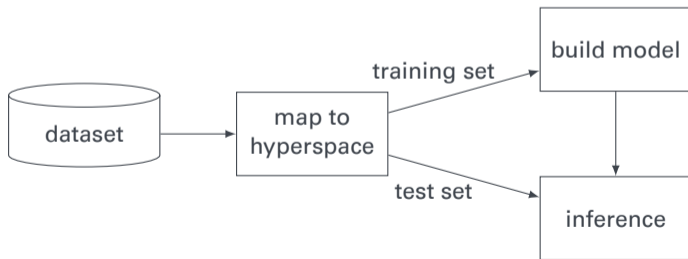
$$A \oplus B = \begin{matrix} -1 & 0 & 1 & 2 \end{matrix}$$

Operation	Symbol	$\cos()$ with input	Implementation
Similarity	$\cos(A, B)$	-	Cosine similarity
Bundle	$A \oplus B$	0.7	component-wise addition
Bind	$A \otimes B$	0.0	component-wise multiplication
Permutation	$p(A)$	0.0	circular shift

Background: Concept of Hyperdimensional Vectors

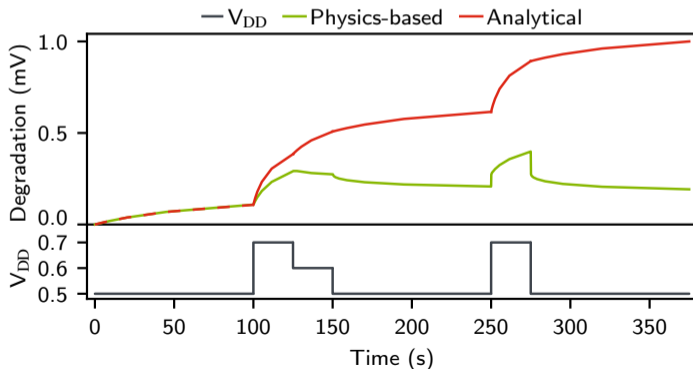
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$$\begin{array}{r} A = 0 \ 1 \ 0 \ 1 \\ B = -1 \ -1 \ 1 \ 1 \\ \hline A \oplus B = -1 \ 0 \ 1 \ 2 \end{array}$$

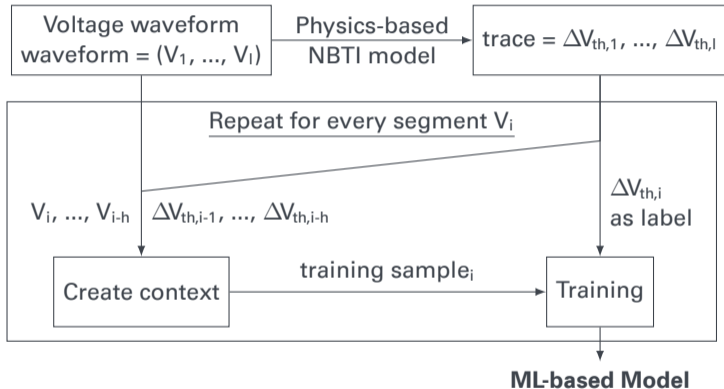


Part I: Brain-inspired Transistor Degradation Model

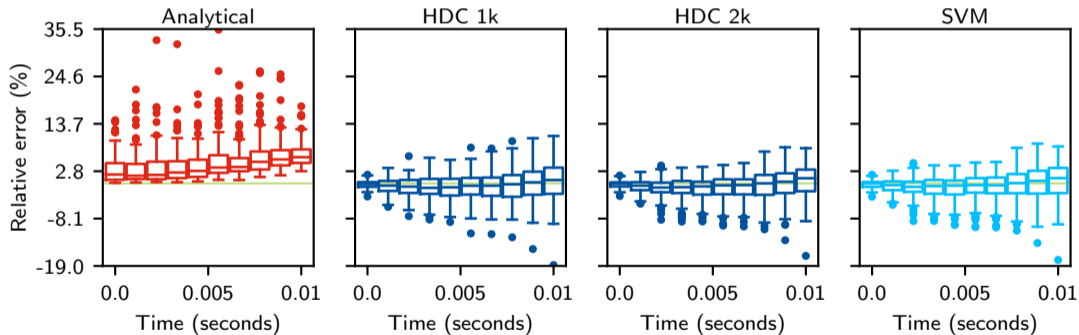
- Predict workload-dependent aging per transistor
- Created by foundry, utilized by circuit designers
- Solves confidentiality problem



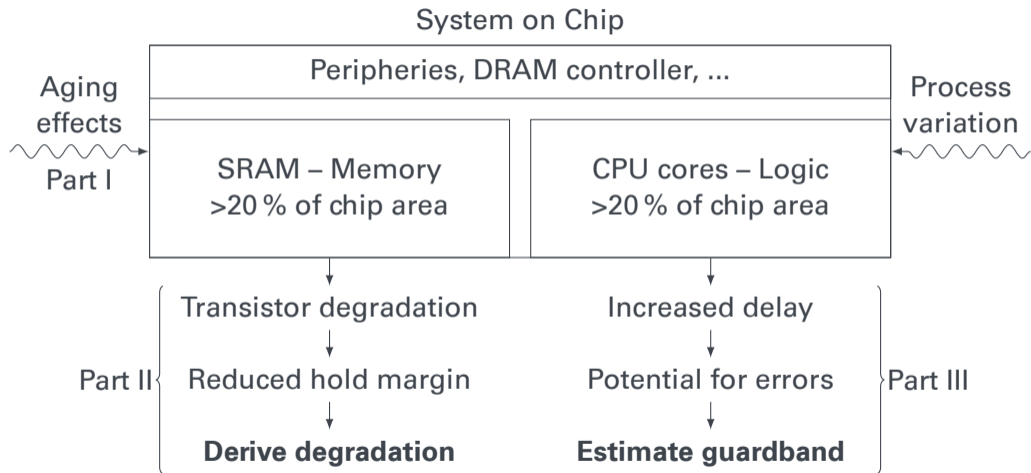
Creating a Brain-inspired Degradation Model



Results for Transistor Degradation Prediction

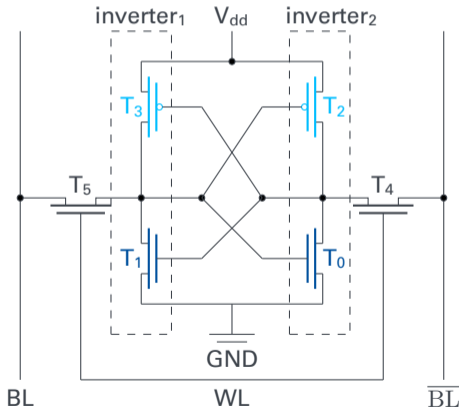


Our Multi-Level Approach



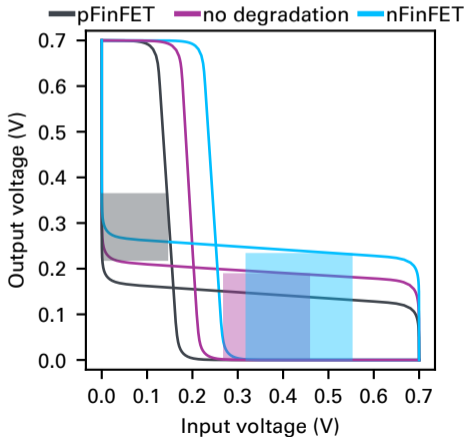
Part II: Noise Resiliency in SRAM

- Dominant on-chip memory
- Static noise margin (SNM)
- Measure “butterfly curve”
- Infer ΔV_{th} through SNM

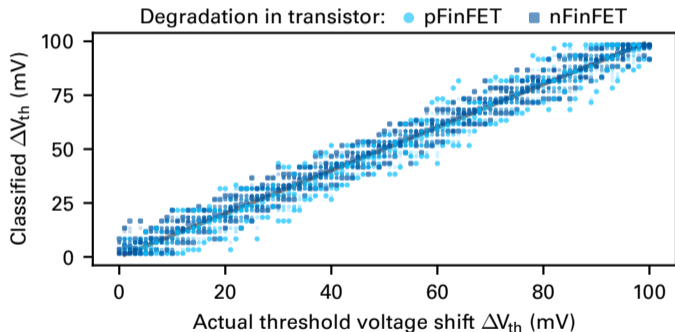


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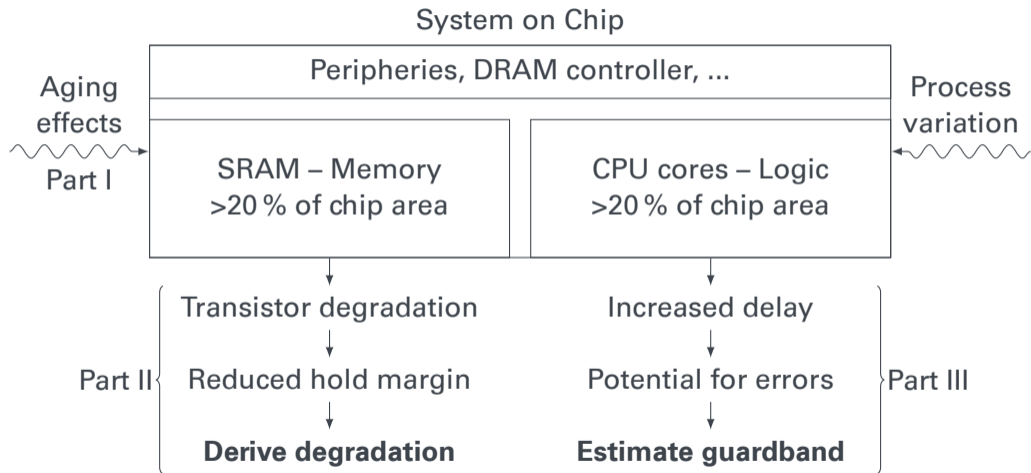
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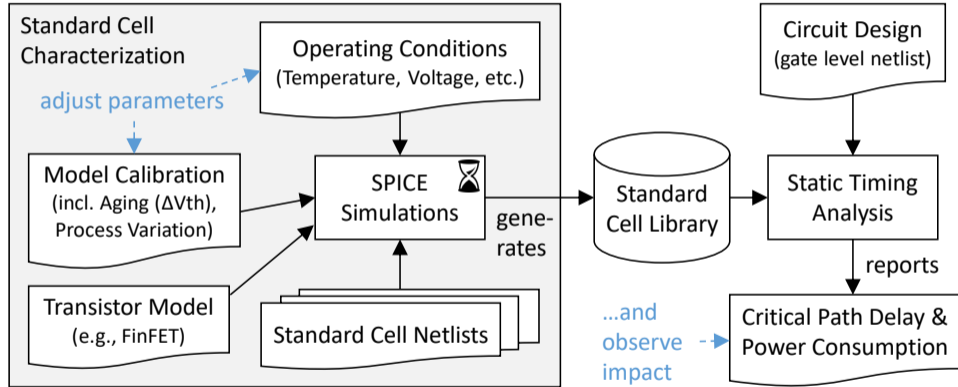
Inferring Degradation through SNM



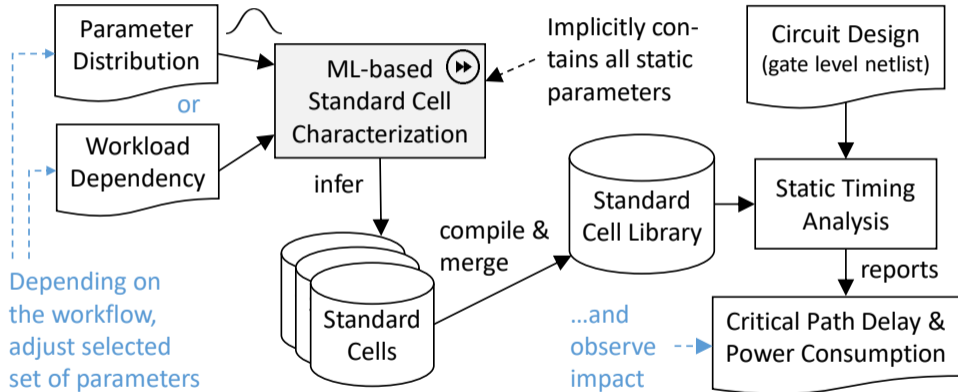
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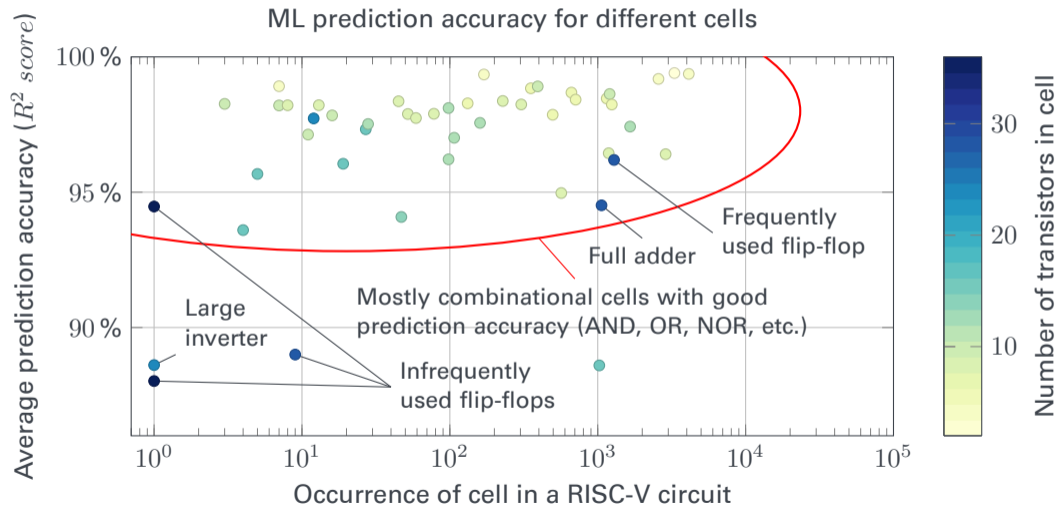
Part III: Cell Library Characterization - Traditional Approach



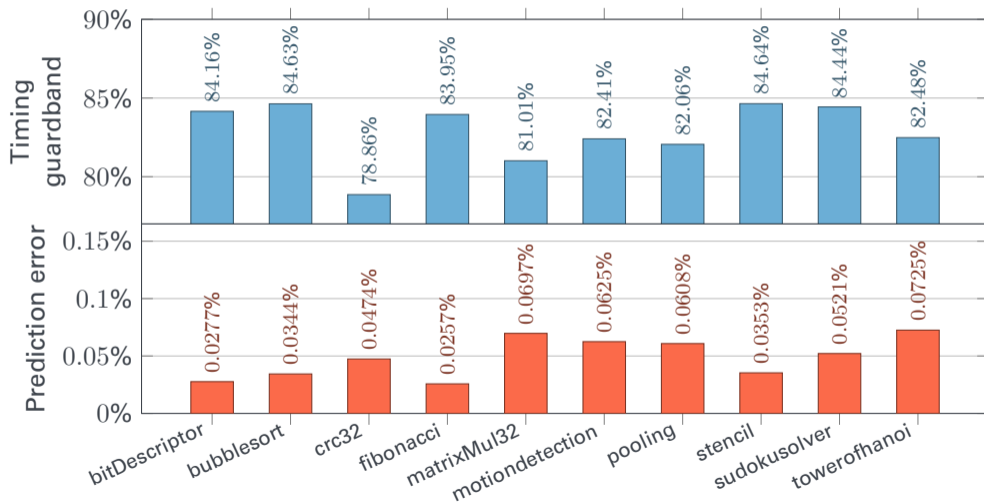
Our ML approach towards Cell Library Characterization



Prediction Results

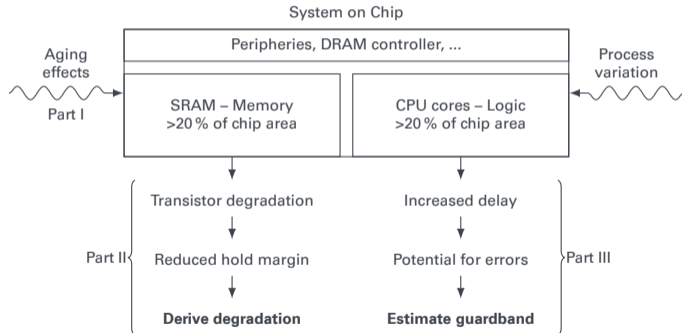


Achievable Timing Guardband Reduction

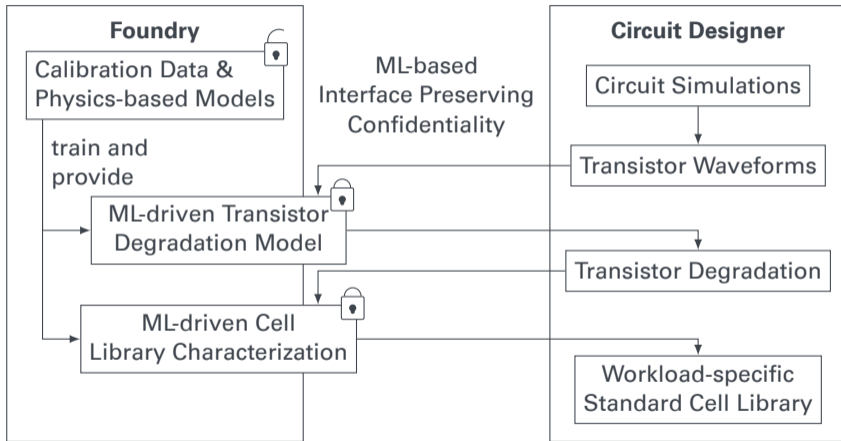


Summary

- Advanced technology challenges pessimistic workflow
- ML-based and brain-inspired methods for close-to-the-edge design



Perspective on ML-based Design Flow





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